Review Questions:

Binary Integer Arithmetic

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- 1. Indicate the decimal value associated with each of the given bit sequences, when the bit sequence is interpreted as an integer number in each of the following representations:
 - a. Unsigned Numbers
 - b. Signed-Magnitude Numbers
 - c. Ones'-Complement Representation
 - d. Two's-Complement Representation
 - e. Saturation Arithmetic
 - f. Excess-2,047
 - g. Excess-2,048
 - (a) 1011001111110₂
 - (b) 010010101100₂
 - (c) 110101110101₂
 - (d) 011100111010₂
 - (e) 101010101100₂
 - (f) 110000111010₂
 - (g) 111001111110₂
 - (h) 100110010101₂
 - (i) 001010011010₂
 - (j) 100011001100₂
- 2. Describe the algorithm for the addition of two Signed-Magnitude binary integers.

3. Fill in the following table, showing the specified values for integer arithmetic of **10-bit** numbers:

Number Representation	Range of Numbers Represented	How many zeroes?	Carry Bit represents Carry-Out from which bit in the Sum Register?	How do you go about finding the representation of the negative of a number?
Unsigned Numbers				
Signed-Magnitude				
Ones'-Complement				
Two's-Complement				
Saturation Arithmetic				
Excess-511				
Excess-512				

Instructions for the Next Several Problems: Add each of the following pairs of binary numbers five times, following the rules of:

- a. Unsigned Numbers
- b. Signed-Magnitude Numbers
- c. Ones'-Complement Representation
- d. Two's-Complement Representation
- e. Saturation Arithmetic

In each case:

- (i) show the carry in for each bit;
- (ii) show the bit sequence that would appear in the Sum Register;
- (iii) indicate what is the decimal value represented by the bit sequence of the Augend;
- (iv) indicate what is the decimal value represented by the bit sequence of the Addend:
- (v) indicate what is the decimal value represented by the bit sequence that would appear in the Sum Register;
- (vi) indicate whether a 0 or a 1 would appear in the Carry Bit of the Status Register:
- (vii) indicate the value (0 or 1) that would appear in the Overflow Bit of the Status Register; and
- (viii) state whether or not the value of the bit sequence appearing in the Sum Register is the correct sum of the values of the numbers represented in the Augend and Addend Registers.

			UN	VSIC	GNE	D II	NTE	GE	RS			
Carry Bits: Decimal Values: Z bit:												
Augend Register: 0 0 1 0 1 1 1 1 N bit:												
Addend Register:	Addend Register: 0											
Sum Register: V bit:												

		SIGN	NED)-M	4GN	JTI	JDE	IN	ΓEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 0 0 1 0 1 1 1 1 N bit:													
Addend Register:	0	1	0	0	1	1	1	0		C bit:			
Sum Register:	Sum Register: V bit:												

		ONE	S'-(CON	1PL	EM]	ENT	IN	ΓEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 0 0 1 0 1 1 1 1 N bit:													
Addend Register:	Addend Register: 0 1 0 0 1 1 0 0 C bit:												
Sum Register: V bit:													

	,	ΓWC)'S-(CON	ИPL	EM	ENT	IN'	TEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 0 0 1 0 1 1 1 1 N bit:													
Addend Register:	0	1	0	0	1	1	1	0		C bit:			
Sum Register:													

		S	ATU	JRA	TIO	N A	RIT	HM	IETIC			
Carry Bits: Decimal Values: Z bit:												
Augend Register: 0 0 1 0 1 1 1 1 N bit:												
Addend Register:	0	1	0	0	1	1	1	0		C bit:		
Sum Register:	Sum Register: V bit:											

			UN	NSIC	GNE	D N	IUM	[BE]	RS			
Carry Bits: Decimal Values: Z bit:												
Augend Register: 0 1 1 0 1 1 1 N bit:												
Addend Register:	0	1	0	0	1	1	1	0		C bit:		
Sum Register: V bit:												

		SIG	NED)-M	AGN	JTI	JDE	IN	ΓEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 0 1 1 0 1 1 1 1 N bit:													
Addend Register:	Addend Register: 0 1 0 0 1 1 0 0 C bit:												
Sum Register: V bit:													

		ONE	S'-(CON	1PL	EMI	ENT	IN	ΓEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 0 1 1 0 1 1 1 1 N bit:													
Addend Register:	Addend Register: 0 1 0 0 1 1 0 0 C bit:												
Sum Register:													

	,	ΓWC)'S-(CON	ЛPL	EM.	ENT	IN'	TEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 0 1 1 0 1 1 1 1 N bit:													
Addend Register:	0	1	0	0	1	1	1	0		C bit:			
Sum Register:	Sum Register: V bit:												

		S	JTA	JRA	TIO	N A	RIT	THM	IETIC				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 0 1 1 0 1 1 1 1 N bit:													
Addend Register:	0	1	0	0	1	1	1	0		C bit:			
Sum Register:	Sum Register: V bit:												

			UN	VSIC	GNE	DN	IUM	[BE]	RS			
Carry Bits: Decimal Values: Z bit:												
Augend Register: 1 0 1 0 1 1 1 1 N bit:												
Addend Register:	0	1	0	0	1	1	1	0		C bit:		
Sum Register: V bit:												

	SIGNED-MAGNITUDE INTEGERS													
Carry Bits: Decimal Values: Z bit:														
Augend Register: 1 0 1 0 1 1 1 1 N bit:														
Addend Register:	0	1	0	0	1	1	1	0		C bit:				
Sum Register:										V bit:				

		ONE	ES'-(CON	1PL	EM]	ENT	IN	ΓEGERS					
Carry Bits: Decimal Values: Z bit:														
Augend Register: 1 0 1 0 1 1 1 1 N bit:														
Addend Register:	Addend Register: 0 1 0 0 1 1 0 0 C bit:													
Sum Register:	Sum Register: V bit:													

	,	ΓWC)'S-(CON	ЛPL	EM	ENT	ΓIN'	TEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 0 1 0 1 1 1 1 N bit:													
Addend Register:	0	1	0	0	1	1	1	0		C bit:			
Sum Register:										V bit:			

		S	ATU	JRA	TIO	N A	RIT	THM	IETIC				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 0 1 0 1 1 1 1 N bit:													
Addend Register:	0	1	0	0	1	1	1	0		C bit:			
Sum Register:										V bit:			

			UN	VSIC	GNE	DN	IUM	[BE]	RS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 0 1 0 1 1 1 1 N bit:													
Addend Register:	1	1	0	0	1	1	1	0		C bit:			
Sum Register:													

		SIG	NED)-M	4GN	JTI	JDE	IN	ΓEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 0 1 0 1 1 1 1 N bit:													
Addend Register:	Addend Register: 1 1 0 0 1 1 1 0 C bit:												
Sum Register:	Sum Register: V bit:												

		ONE	S'-(CON	1PL	EMI	ENT	IN	ΓEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 0 1 0 1 1 1 1 N bit:													
Addend Register:													
Sum Register:	<u> </u>												

	,	TWC)'S-(CON	ИPL	EM	ENT	IN'	TEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 0 1 0 1 1 1 1 N bit:													
Addend Register: 1 1 0 0 1 1 1 0 C bit:													
Sum Register:										V bit:			

		S	ATL	JRA	TIO	N A	RIT	HM	IETIC			
Carry Bits: Decimal Values: Z bit:												
Augend Register: 1 0 1 0 1 1 1 1 N bit:												
Addend Register:	Addend Register: 1											
Sum Register:	Sum Register: V bit:											

			UN	NSIC	GNE	DN	IUM	[BE]	RS			
Carry Bits: Decimal Values: Z bit:												
Augend Register: 1 1 1 0 1 1 1 1 N bit:												
Addend Register:	Addend Register: 1 1 0 0 1 1 0 0 C bit:											
Sum Register: V bit:												

CICNED MACNITUDE INTECEDO														
	SIGNED-MAGNITUDE INTEGERS													
Carry Bits: Decimal Values: Z bit:														
Augend Register: 1 1 1 0 1 1 1 1 N bit:														
Addend Register:	1	1	0	0	1	1	1	0		C bit:				
Sum Register:	<u> </u>													

		ONE	ES'-(CON	1PL	EM]	ENT	IN	ΓEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 1 1 0 1 1 1 1 N bit:													
Addend Register:	1	1	0	0	1	1	1	0		C bit:			
Sum Register:	Sum Register: V bit:												

	,	TWC)'S-(CON	ИPL	EM	ENT	ΓΙΝ	TEGERS				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 1 1 0 1 1 1 1 N bit:													
Addend Register:													
Sum Register:													

		SA	ATU	JRA	TIO	N A	RIT	HM	IETIC				
Carry Bits: Decimal Values: Z bit:													
Augend Register: 1 1 1 0 1 1 1 1 N bit:													
Addend Register:	1	1	0	0	1	1	1	0		C bit:			
Sum Register:	Sum Register: V bit:												

Answers to Selected Questions:

Question 1:

(a) 101100111110₂

Ones'-Complement: a negative number, whose complement is : 010011000001_2 or 1,217. Thus, the value of the original bit sequence is -1,217.

Two's Complement: a negative number, which when first complemented and then incremented comes out to 010011000010₂ or 1,218. Thus, the value of the original bit sequence is —1,218.

Saturation Arithmetic: Same value as for Unsigned Numbers: 2,878.

(b) 010010101100₂

Since the MSB is zero, this number represents the same value in all of the representation schemes listed: 0 + 0 + 4 + 8 + 0 + 32 + 0 + 128 + 0 + 0 + 1,024 = 1,196

(c) 110101110101₂

Unsigned Number: 1 + 0 + 4 + 0 + 16 + 32 + 64 + 0 + 256 + 0 + 1,024 + 2,048 = 3,445Signed-Magnitude: negative sign bit, magnitude 1 + 0 + 4 + 0 + 16 + 32 + 64 + 0 + 256 + 0 + 1,024, thus representing —1,397

Ones' Complement: a negative number, whose complement is 001010001010_2 or 740. Thus, the value of the original bit sequence is -650.

Two's Complement: a negative number which when first complemented and then incremented comes out to 001010001011₂ or 651. Thus, the value of the original bit sequence is —651.

Saturation Arithmetic: Same value as for Unsigned Numbers: 3,445.

(d) 011100111010₂

Since the MSB is zero, this number represents the same value in all of the representation schemes listed: 0 + 2 + 0 + 8 + 16 + 32 + 0 + 0 + 256 + 512 + 1,024 = 1,850

(e) 101010101100₂

Unsigned Number: 0 + 0 + 4 + 8 + 0 + 32 + 0 + 128 + 0 + 512 + 0 + 2,048 = 2,732

- Signed-Magnitude: negative sign bit, magnitude 0 + 0 + 4 + 8 + 0 + 32 + 0 + 128 + 0 + 512 + 0, thus representing —684.
- Ones' Complement: a negative number, whose complement is 0101010101011_2 or 1,363. Thus, the value of the original bit sequence is -1,363.
- Two's Complement: a negative number which when first complemented and then incremented comes out to 010101010100_2 or . Thus, the value of the original bit sequence is -.1,364

Saturation Arithmetic: Same value as for Unsigned Numbers: 2,732.

(f) 110000111010₂

Unsigned Number: 0+2+0+8+16+32+0+0+0+0+1,024+2,048=3,130Signed-Magnitude: negative sign bit, magnitude 0+2+0+8+16+32+0+0+0+0+1,024, thus representing —1,082.

Ones' Complement: a negative number, whose complement is 001111000101_2 or 965. Thus, the value of the original bit sequence is --965.

Two's Complement: a negative number which when first complemented and then incremented comes out to 001111000110₂ or 966. Thus, the value of the original bit sequence is —966.

Saturation Arithmetic: Same value as for Unsigned Numbers: 3,130.

(g) 111001111110₂

Unsigned Number: 0 + 2 + 4 + 8 + 16 + 32 + 64 + 0 + 0 + 512 + 1,024 + 2,048 = 3,710Signed-Magnitude: negative sign bit, magnitude 0 + 2 + 4 + 8 + 16 + 32 + 64 + 0 + 0 + 512 + 1,024, thus representing —1,662.

Ones' Complement: a negative number, whose complement is 000110000001_2 or 385. Thus, the value of the original bit sequence is -385.

Two's Complement: a negative number which when first complemented and then incremented comes out to 000110000010_2 or 386. Thus, the value of the original bit sequence is —386.

Saturation Arithmetic: Same value as for Unsigned Numbers: 3,710.

(h) 100110010101₂

Unsigned Number: 1+0+4+0+16+0+0+128+256+0+0+2,048=2,453Signed-Magnitude: negative sign bit, magnitude 1+0+4+0+16+0+0+128+256+0+0+0, thus representing —405.

Ones' Complement: a negative number, whose complement is 011001101010_2 or 1,642. Thus, the value of the original bit sequence is -1,642.

Two's Complement: a negative number which when first complemented and then incremented comes out to 011001101011₂ or 1,643. Thus, the value of the original bit sequence is —1,643.

Saturation Arithmetic: Same value as for Unsigned Numbers: 2,453.

(i) 001010011010₂

Since the MSB is zero, this number represents the same value in all of the representation schemes listed: 0 + 2 + 0 + 8 + 16 + 0 + 0 + 128 + 0512 = 666

(j) 100011001100₂

Unsigned Number: 0+0+4+8+0+0+64+128+0+0+0+2,048 = 2,252Signed-Magnitude: negative sign bit, magnitude = 0+0+4+8+0+0+64+128+0+0+0+0, thus representing —204.

Ones' Complement: a negative number, whose complement is 011100110011_2 or 1,843. Thus, the value of the original bit sequence is -1,843.

Two's Complement: a negative number which when first complemented and then incremented comes out to 011100110100₂ or 1,844. Thus, the value of the original bit sequence is —1,844.

Saturation Arithmetic: Same value as for Unsigned Numbers: 2,252.

Question 2: (i) Are the sign bits identical or different?

- (iia) Identical: Replicate the common sign bit in the sum register.
- (iiia) Add the magnitude bits of the augend and the addend to obtain the magnitude bits of the sum.
- (iva) In case of overflow, set the V bit; otherwise, clear it.
- (iib) Different: Determine which number has the larger magnitude, and replicate its sign bit in the sum register.
- (iiib) Subtract the magnitude of the smaller number from the magnitude of the larger number; the difference goes into the magnitude field of the sum register.
- (ivb) Clear the *V* bit.

Question 3:

Number Representation	Range of Numbers Represented	How many zeroes?	Carry Bit represents Carry-Out from which bit in the Sum Register?	How do you go about finding the representation of the negative of a number?
Unsigned Numbers	$\theta \rightarrow 1,023$	1	Bit 10	not applicable
Signed-Magnitude	<i>-511</i> → + <i>511</i>	2	Bit 9	Invert the sign bit (bit 10).
Ones'-Complement	<i>-511</i> → + <i>511</i>	2	Bit 10	Complement the number (1s'-complement).
Two's-Complement	<i>-512</i> → <i>+511</i>	1	Bit 10	Complement the number (1s'-complement), and then increment it. The result is the 2's-complement. Of the number.
Saturation Arithmetic	$\theta \rightarrow 1,023$	1	not applicable	not applicable
Excess-511	<i>-511</i> → <i>+512</i>	1	not applicable	Add 511 to the number, and represent the sum as an "Unsigned" (Non-explicitly-Signed) Number.
Excess-512	<i>-512</i> → <i>+511</i>	1	not applicable	Add 512 to the number, and represent the sum as an "Unsigned" (Non-explicitly-Signed) Number.

Question 4:

			UN	VSIC	GNE	D II	NTE	GEI	RS				
Carry Bits: 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register:	Augend Register: 0 0 1 0 1 1 1 1 +47 N bit: 0												
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0		
Sum Register:	0	1	1	1	1	1	0	1	+125	V bit:	0		

Correct sum

		SIG	NED	-M	4GN	JTI	JDE	IN	ΓEGERS				
Carry Bits: 0 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register: 0 0 1 0 1 1 1 1 +47 N bit: 0													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0		
Sum Register:	0	1	1	1	1	1	0	1	+125	V bit:	0		

Correct sum

		ONE	S'-(CON	1PL	EM	ENT	IN	ΓEGERS					
Carry Bits:	Carry Bits: 0 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register:	Augend Register: 0 0 1 0 1 1 1 1 +47 N bit: 0													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0			
Sum Register:	0	1	1	1	1	1	0	1	+125	V bit:	0			

Correct sum

	r	ΓWC	'S-(CON	ЛPL	EM.	ENT	ſ IN	TEGERS				
Carry Bits: 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register: 0 0 1 0 1 1 1 1 +47 N bit: 0													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0		
Sum Register:	0	1	1	1	1	1	0	1	+125	V bit:	0		

Correct sum

		S	ATU	JRA	TIO	N A	RIT	THM	IETIC				
Carry Bits: 0 0 0 1 1 1 0 0 Decimal Values: Z bit:													
Augend Register: 0 0 1 0 1 1 1 1 +47 N bit:													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:			
Sum Register:	0	1	1	1	1	1	0	1	+125	V bit:			

Correct sum

Question 5:

			UN	ISIC	GNE	DN	IUM	[BE]	RS			
Carry Bits: 1 0 0 1 1 1 0 0 Decimal Values: Z bit: 0												
Augend Register:	Augend Register: 0 1 1 0 1 1 1 1 +111 N bit: 0											
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0	
Sum Register:	1	0	1	1	1	1	0	1	+189	V bit:	0	

Correct sum

		SIG	NED	-M	AGN	JTI	JDE	IN	ΓEGERS				
Carry Bits: X 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register: 0 1 1 0 1 1 1 1 +111 N bit: 0													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	1		
Sum Register:													

Not the correct sum (Overflow)

		ONE	S'-(CON	1PL	EMI	ENT	IN	ΓEGERS					
Carry Bits:														
Augend Register:	Augend Register: 0 1 1 0 1 1 1 1 +111 N bit: 0													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0			
Sum Register:	1	0	1	1	1	1	0	1	-66	V bit:	1			

Not the correct sum (Overflow)

	r	ΓWC)'S-(CON	ЛPL	EM.	ENT	ſ IN	TEGERS				
Carry Bits: 1 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register: 0													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0		
Sum Register:	1	0	1	1	1	1	0	1	-67	V bit:	1		

Not the correct sum (Overflow)

		S	ATL	JRA	TIO	N A	RIT	THM	IETIC				
Carry Bits: 1 0 0 1 1 1 0 1 Decimal Values: Z bit:													
Augend Register: 0 1 1 0 1 1 1 1 +111 N bit:													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:			
Sum Register:	1	0	1	1	1	1	0	1	+189	V bit:			

Correct sum

Question 6:

			UN	ISIC	GNE	DN	IUM	[BE]	RS				
Carry Bits: 0 0 0 1 1 1 0 1 Decimal Values: Z bit: 0													
Augend Register: 1 0 1 0 1 1 1 1 +175 N bit: 0													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0		
Sum Register:	1	1	1	1	1	1	0	1	+253	V bit:	0		

Correct sum

		SIG	NED)-M	AGN	JTI	JDE	IN	ΓEGERS				
Carry Bits: X 1 1 1 1 1 1 O Decimal Values: Z bit: 0													
Augend Register:	Augend Register: 1 0 1 0 1 1 1 1 -47 Nbit: 0												
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0		
Sum Register:	Sum Register: 0 0 0 1 1 1 1 1 +31 V bit: 0												

Correct sum

		ONE	S'-(CON	1PL	EM	ENT	IN	ΓEGERS				
Carry Bits: 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register: 1 0 1 0 1 1 1 1 -80 N bit: 1													
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0		
Sum Register:	1	1	1	1	1	1	0	1	-2	V bit:	0		

Correct sum

	,	TWC)'S-(CON	ИPL	EM	ENT	ΓΙΝ΄	TEGERS					
Carry Bits: 0 0 0 1 1 1 0 1 Decimal Values: Z bit: 0														
Augend Register: 1 0 1 0 1 1 1 1 -81 N bit: 1														
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:	0			
Sum Register:	1	1	1	1	1	1	0	1	-3	V bit:	0			

Correct sum

	SATURATION ARITHMETIC													
Carry Bits: 0 0 0 1 1 1 0 0 Decimal Values: Z bit:														
Augend Register: 1 0 1 0 1 1 1 1 +175 N bit:														
Addend Register:	0	1	0	0	1	1	1	0	+78	C bit:				
Sum Register: 1														

Correct sum

Question 7:

			UN	ISIC	GNE	DN	IUM	[BE]	RS				
Carry Bits: 0 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register:													
Addend Register:	1	1	0	0	1	1	1	0	+206	C bit:	1		
Sum Register:	Sum Register: 0												

Not the correct sum (Overflow)

		SIG	NED)-M	AGN	JTI	JDE	IN	ΓEGERS				
Carry Bits: X 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register:													
Addend Register:	1	1	0	0	1	1	1	0	-78	C bit:	0		
Sum Register:													

Correct sum

		ONE	S'-(CON	1PL	EMI	ENT	IN	ΓEGERS				
Carry Bits: 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register:													
Addend Register:	1	1	0	0	1	1	1	0	-49	C bit:	1		
Sum Register:	0	1	1	1	1	1	0	1	+125	V bit:	1		

Not the correct sum (Overflow)

	r	ΓWC)'S-(CON	ЛPL	EM.	ENT	IN'	TEGERS				
Carry Bits: 0 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register:													
Addend Register:	1	1	0	0	1	1	1	0	-50	C bit:	1		
Sum Register:	0	1	1	1	1	1	0	1	+125	V bit:	1		

Not the correct sum (Overflow)

		$\mathbf{S}_{\mathbf{A}}$	ATL	JRA	TIO	N A	RIT	THM	IETIC				
Carry Bits: 0 0 1 1 1 0 0 Decimal Values: Z bit:													
Augend Register: 1 0 1 0 1 1 1 1 +175 N bit:													
Addend Register:	1	1	0	0	1	1	1	0	+206	C bit:			
Sum Register:	1	1	1	1	1	1	1	1	+255	V bit:			

Correct sum, in accordance with the rules of Saturation Arithmetic!

Question 8:

			UN	NSIC	GNE	DN	IUM	[BE]	RS				
Carry Bits: 1 0 0 1 1 1 0 0 Decimal Values: Z bit: 0													
Augend Register:													
Addend Register:	1	1	0	0	1	1	1	0	+206	C bit:	1		
Sum Register:													

Not the correct sum

SIGNED-MAGNITUDE INTEGERS											
Carry Bits: 1 0 0 1 1 1 0 0 Decimal Values: Z bit: 0											
Augend Register:	1	1	1	0	1	1	1	1	-111	N bit:	1
Addend Register:	1	1	0	0	1	1	1	0	-78	C bit:	1
Sum Register:	1	0	1	1	1	1	0	1	-61	V bit:	1

Not the correct sum

ONES'-COMPLEMENT INTEGERS											
Carry Bits:	1	0	0	1	1	1	0	0	Decimal Values:	Z bit:	0
Augend Register:	1	1	1	0	1	1	1	1	-16	N bit:	1
Addend Register:	1	1	0	0	1	1	1	0	-49	C bit:	1
Sum Register:	1	0	1	1	1	1	0	1	-66	V bit:	0
Incremented Sum	1	0	1	1	1	1	1	0	-65		

An additional operation (End-Around Carry) needs to be performed before the value in the sum register becomes equal to the true sum of the numbers (Ones'-Complement arithmetic).

TWO'S-COMPLEMENT INTEGERS											
Carry Bits:	1	0	0	1	1	1	0	0	Decimal Values:	Z bit:	0
Augend Register:	1	1	1	0	1	1	1	1	-17	N bit:	1
Addend Register:	1	1	0	0	1	1	1	0	-50	C bit:	1
Sum Register:	1	0	1	1	1	1	0	1	-67	V bit:	0

Correct sum

SATURATION ARITHMETIC										
Carry Bits:	1	0	0	1	1	1	0	0	Decimal Values:	Z bit:
Augend Register:	1	1	1	0	1	1	1	1	+239	N bit:
Addend Register:	1	1	0	0	1	1	1	0	+206	C bit:
Sum Register:	1	1	1	1	1	1	1	1	+255	V bit:

Correct sum, in accordance with the rules of Saturation Arithmetic!