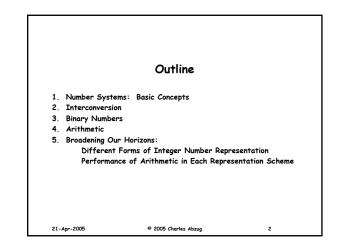
# CS-228: Discrete Structures II: REPRESENTATION of NUMBERS in DIGITAL COMPUTERS

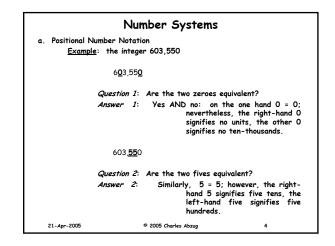
*Charles Abzug, Ph.D.* Department of Computer Science James Madison University Harrisonburg, VA 22807

Voice Phone: 540-568-8746; Cell Phone: 443-956-9424 E-mail: abzugcx@JMU.edu OR CharlesAbzug@ACM.org Home Page: http://www.cs.jmu.edu/users/abzugcx

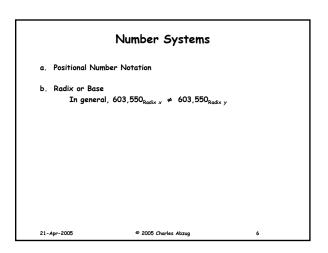
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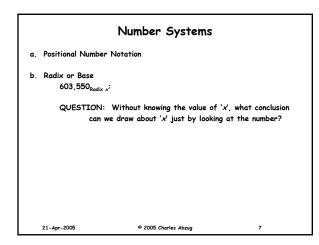


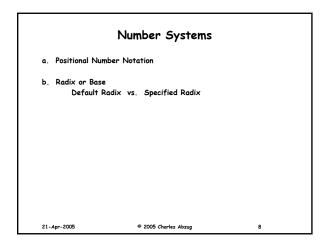
a. Positional Number Notati <u>Example</u> : the intege	er 603,550	
6 <u>0</u> 3,55 <u>0</u>		
Question 1:	Are the two zeroes equivalent?	
603, <u>55</u> 0	,	
Question 2:	Are the two fives equivalent?	
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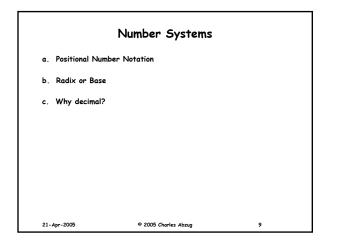


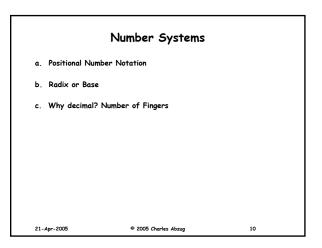
	Number Systems	
a. Positional Num	ber Notation	
b. Radix or Base		
Example <sub>1</sub> :	$603,550_{10} = 0 \times 10^{0} +$	
	5 x 10 <sup>1</sup> +	
	5 x 10 <sup>2</sup> +	
	3 × 10 <sup>3</sup> +	
	0 x 10 <sup>4</sup> +	
	6 × 10 <sup>5</sup>	
Example <sub>2</sub> :	$603,550_{16} = 0 \times 16^{\circ} +$	
	5 × 16 <sup>1</sup> +	
	5 x 16 <sup>2</sup> +	
	3 x 16 <sup>3</sup> +	
	0 x 16 <sup>4</sup> +	
	6 × 16 <sup>5</sup> = 3,90	5,404 <sub>10</sub>
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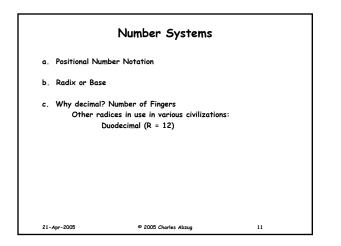


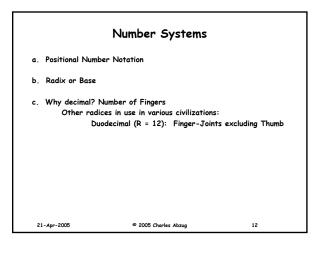


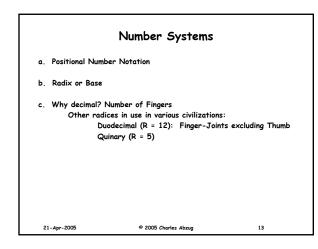


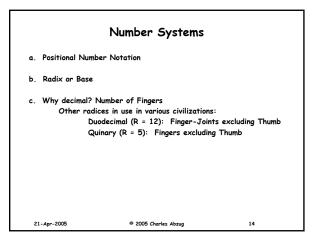


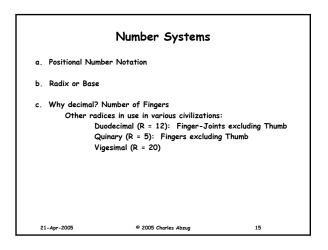


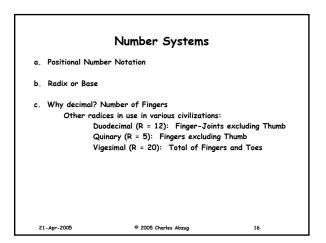


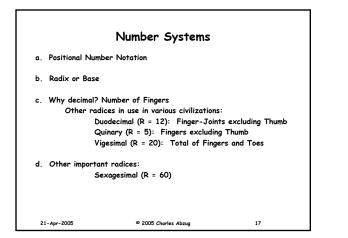


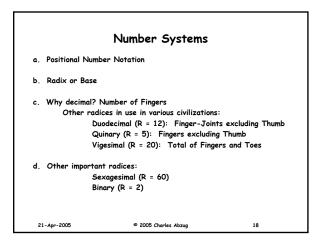


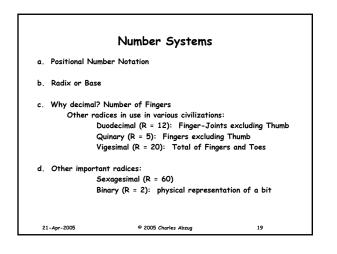


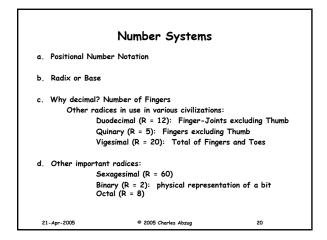


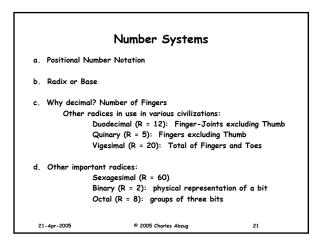


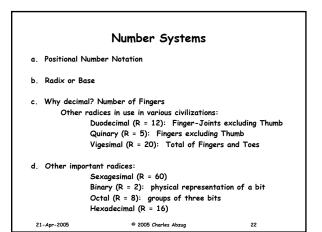










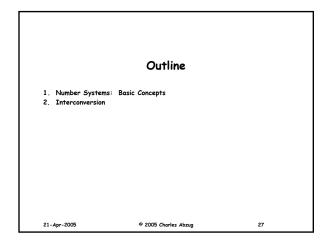


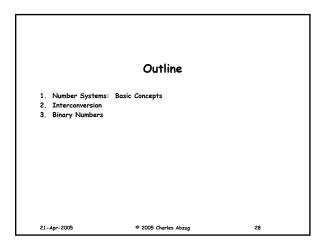
	Number Systems	
a. Positional I	Number Notation	
b. Radix or B	ase	
· · ·	al? Number of Fingers radices in use in various civilizations Duodecimal (R = 12): Finger-Joint Quinary (R = 5): Fingers excluding Vigesimal (R = 20): Total of Finge	rs excluding Thumb g Thumb
d. Other impo	ortant radices: Sexagesimal (R = 60) Binary (R = 2): physical represent Octal (R = 8): groups of three bit Hexadecimal (R = 16): groups of f	ts
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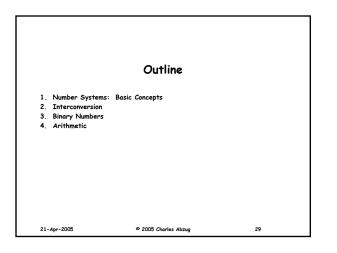
	Number Sy	stems
a. Positional Numbe	r Notation	
b. Radix or Base		
c. Why decimal?		
d. Other important	radices	
We are NOT limited	to integers:	
e. Rational Number "Rea		erminology) ≡ outer science terminology)
Fractional N	lumbers: e.g.,	1,941/10,000 = 0.194
"Mixed" Nur	nbers: e.g.,	603,550.1941

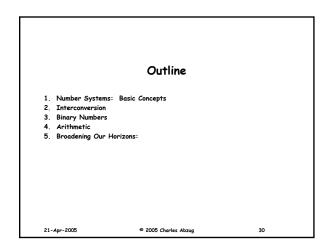
Fr	Fractional Numbers							
DECIMAL NUMBERS:								
Decimal Point	603,550.1941							
NUMBERS OF VARIOU	S RADICES:							
Radix Point	603,550.1941 <sub>11</sub>	603,550.1941 <sub>13</sub>						
	603,550.1941 <sub>26</sub>	603,550.1941 <sub>18</sub>						
SPECIFIC RADICES:								
Binary Point:	1011 1101 0101.110	00 1001 0001 <sub>2</sub>						
Octal Point:	7214.365	502 <sub>8</sub>						
Hexadecimal P	oint: FEED37.098	BADE <sub>16</sub>						
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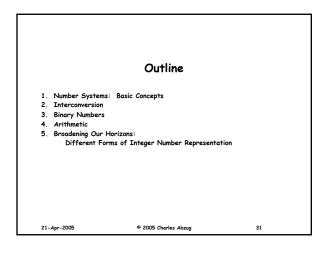
	Outline	
1. Number Systems:	Basic Concepts	
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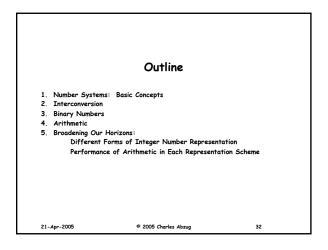












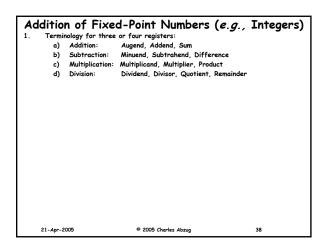
Multiplication			Computer Science	
Factor in non-CS Scientific Notation	Name	Sym- bol	Multipli- cation Factor	Magnitude
10 <sup>3</sup>	kilo	k	210	1,024
106	Mega	M	2 <sup>20</sup>	1,048,576
10 <sup>9</sup>	Giga	G	2 <sup>30</sup>	1,073,741,824
1012	Tera	т	240	1,099,511,627,776
10 <sup>15</sup>	Peta	Р	2 <sup>50</sup>	1,125,899,906,842,624
1018	E×α	E	260	1,152,921,504,606,846,976
10 <sup>21</sup>	Zetta	z	270	1,180,591,620,717,411,303,424
10 <sup>24</sup>	Yotta	У	280	1,208,925,819,614,629,174,706,176

Multiplication Factor				Computer Science	
in non-CS Scientific Notation	Name	Sym- bol	Multipli- cation Factor	Magnitude	
10-3	milli	m	2-10	1.0/1,024	
10-6	micro	μ	2 <sup>-20</sup>	1.0/1,048,576	
10-9	nano	n	2 <sup>-30</sup>	1.0/1,073,741,824	
10-12	pico	р	2 <sup>-40</sup>	1.0/1,099,511,627,776	
10-15	femto	f	2 <sup>-50</sup>	1.0/1,125,899,906,842,624	
10 <sup>-18</sup>	atto	۵	2-60	1.0/1,152,921,504,606,846,976	
10-21	zepto	z	2-70	1.0/1,180,591,620,717,411,303,424	
10-24	yocto	у	2-80	1.0/1,208,925,819,614,629,174,706,176	

Dubious	s Me	etrics
Base Quantity		Equivalent
10^12 dactyls	=	1 teradactyl
10^21 piccolos	=	1 gigolo
10^6 airs	=	1 millionair
10^-12 dillies	=	1 picodilly
10 <sup>12</sup> bulls	=	1 terabull
2x10^3 mockingbirds	=	2 kilo mockingbird

Repres	sentation	Dec	imal Value Re	presented	
Hex	Binary	Unsigned (Non- Explicitly-Signed)	Ones' Complement	Two's Complement	Signed- Magnitude
0	0000	0	+0	0 ("+"0)	+0
1	0001	1	+1	+1	+1
2	0010	2	+2	+2	+2
3	0011	3	+3	+3	+3
4	0100	4	+4	+4	+4
5	0101	5	+5	+5	+5
6	0110	6	+6	+6	+6
7	0111	7	+7	+7	+7
8	1000	8	-7	-8	-0
9	1001	9	-6	-7	-1
Α	1010	10	-5	-6	-2
В	1011	11	-4	-5	-3
С	1100	12	-3	-4	-4
D	1101	13	-2	-3	-5
E	1110	14	-1	-2	-6
F	1111	15	-0	-1	-7
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	Repres	sentation	Decimal Val	ue Represer	nted
	Hex	Binary	Unsigned (Non- Explicitly-Signed)	Excess-7	Excess-8
	0	0000	0	-7	-8
	1	0001	1	-6	-7
	2	0010	2	-5	-6
	3	0011	3	-4	-5
	4	0100	4	-3	-4
	5	0101	5	-2	-3
	6	0110	6	-1	-2
	7	0111	7	0 ("+"0)	-1
	8	1000	8	+1	0 ("+"0)
	9	1001	9	+2	+1
	Α	1010	10	+3	+2
	В	1011	11	+4	+3
	С	1100	12	+5	+4
	D	1101	13	+6	+5
	E	1110	14	+7	+6
	F	1111	15	+8	+7
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Ad	ditio	n of Fixe	d-Point Numbers (a	e.g., Integers)		
1.			or four registers:			
	a)	Addition:	Augend, Addend, Sum			
	ь)	Subtraction:	n: Minuend, Subtrahend, Difference			
	c)	Multiplication:	Multiplicand, Multiplier, Product	•		
	d)	Division:	Dividend, Divisor, Quotient, Re	mainder		
2.	Rules	for single-bit ad	dition			
	2.	0 + 0 + 0 =	0 (sum), plus 0 (carry in to next	bit)		
	3.	0 + 0 + 1 =	0 + 1 + 0 = 1 + 0 + 0 = 1 (s plus 0 (carry OUT from becomes the ca			
	4.	0 + 1 + 1 =	1 + 1 + 0 = 1 + 0 + 1 = 0 (s plus 1 (carry OUT from becomes the ca			
	5.	1 + 1 + 1 =	1 (sum), plus 1 (carry OUT from becomes the ca	the current bit, which rry in to the next bit)		
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1.	Termi	nology for three	or four registers:	
	a)	Addition:	Augend, Addend, Sum	
	ь)	Subtraction:	Minuend, Subtrahend, Differe	nce
	c)	Multiplication:	Multiplicand, Multiplier, Produc	:t
	d)	Division:	Dividend, Divisor, Quotient, R	emainder
2.	Rules	for single-bit a	ddition	
	a)	0 + 0 + 0 =	0 (sum), plus 0 (carry in to nex	t bit)
	ь)	0 + 0 + 1 =	0 + 1 + 0 = 1 + 0 + 0 = 1 ( plus 0 (carry OUT from becomes the c	
	c)	0 + 1 + 1 =	1 + 1 + 0 = 1 + 0 + 1 = 0 ( plus 1 (carry OUT from becomes the c	
	d)	1 + 1 + 1 =	1 (sum), plus 1 (carry OUT from becomes the c	n the current bit, which arry in to the next bit)
3.	Four s	s <i>tatus bits</i> to as	sist in programming:	
	a)	C: <u>C</u> arry out	from MSB (Most Significant Bit	) of the Sum.
	ь)	Z: Sum has a	value of <u>Z</u> ero.	
	c)	N: Content o	f the Sum Register is a <u>N</u> egative	e number.
	d)	V: Result of	the arithmetic operation is an o	lerflow.
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ASL Mnemonic	Meaning of the Mnemonic	Function
JC	Jump on Carry	If the 'C' bit is a <u>1</u> , then skip to a specified location instead of executing the next instruction
JNC	Jump on NOT Carry	If the 'C' bit is a <u>0</u> , then skip to a specified location instead of executing the next instruction
JZ	Jump on Zero	If the 'Z' bit is a <u>1</u> , then skip to a specified location instead of executing the next instruction
JNZ	Jump on NOT Zero	If the 'Z' bit is a <u>0</u> , then skip to a specified location instead of executing the next instruction
JN	Jump on Negative	If the 'N' bit is a <u>1</u> , then skip to a specified location instead of executing the next instruction
JNN	Jump on <i>NOT</i> Negative	If the 'N' bit is a <u>O</u> , then skip to a specified location instead of executing the next instruction
JV	Jump on oVerflow	If the 'V' bit is a <u>1</u> , then skip to a specified location instead of executing the next instruction
JNV	Jump on <i>NOT</i> oVerflow	If the 'V' bit is a <u>O</u> , then skip to a specified location instead of executing the next instruction

0	RGANIZATION of the SLI	DES
shall be examini Addends. We s	nt and continuing for a substantial ng several different pairs of 8-b hall be adding each Augend-Adde five different types of arithmetic	bit Augends and 8-bit and pair in accordance
• Ones'-Co • Two's-Co • Signed-N	-Number (Non-Explicitly-Signed-N omplement Arithmetic omplement Arithmetic Aggnitude Arithmetic on Arithmetic	lumber) Arithmetic
are equally appli arbitrarily large	e same principles demonstrated he icable to words of any width, fr number of bits, although today th that is a power of two (4-bit, i bit).	rom 2 bits up to any almost all processors
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		FI	RST	' Au	igen	d-A	dde	nd	Pair		
				n		r.					
Aug	gend Register	0	0	1	0	1	1	1	1		
Add	dend Register	0	1	0	0	1	1	1	0		
	Sum Register										
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"UNSIGN				up Exp		•			INTEG	ER
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register										v
									I	· · · · ·
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	2.	Ca	rry	out	the	ор	erat	tion		
"UNSIGN	ED"	' (N	on-l	Exp	licit	ly-S	Sign	ed)	INTEG	ER
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		v
			1			1			1	<u>  •  </u>
21-Apr-2005			0	2005 C	harles d	Abzug			45	

"UNSIGN	ED Bit 8	Bit 7	Bit 6	Expi Bit 5	Bit 4	Bit 3	<u> </u>	Bit 1		51	tatus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	0
Augend Register	0	0	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	0
Sum Register	0	1	1	1	1	1	0	1		v	0
21-Apr-2005				2005 <i>C</i> I	harles /	Abzug			46		

"UNSIGN	ED"	(N	on-l	Expl	icit	ly-S	bign	ed)	INTEG	ER	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits	0	0	0	1	1	1	0	0		C	0
Augend Register	0	0	1	0	1	1	1	1	(+)47	z	0
Addend Register	0	1	0	0	1	1	1	0	(+)78	Ν	0
Sum Register	0	1	1	1	1	1	0	1	(+)125	v	0
21-Apr-2005			0	2005 C	norles d	bzug			47		

ONES'-COMPLEMENT														
Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 2Bit 1Decimal StatuStatu														
Carry-In Bits										С				
Augend Register	0	0	1	0	1	1	1	1		z				
Addend Register	0	1	0	0	1	1	1	0		N				
Sum Register										v				
Sum Register										V				

		ONE	s'-	-CO	MPL	EM	ENT			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		V
			-	2005 <i>C</i> I					49	

		ONE	:5'-	-CO	MPL	.EW	ENI				
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
	-		-	-	· ·	-	-	-	value		
Carry-In Bits	0	0	0	1	1	1	0	0		С	0
Augend Register	0	0	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	0
Sum Register	0	1	1	1	1	1	0	1		V	0
OTE that <u>BOTH</u> th the Sum Regis											tent

	(	ONE	s'-	CO	MPL	.EMI	ENT	-			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits	0	0	0	1	1	1	0	0		С	0
Augend Register	0	0	1	0	1	1	1	1	+47	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	0
Sum Register	0	1	1	1	1	1	0	1	+125	v	0
									1		

		W	13	-20	MPL	-CW	CIN	I		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register										v

	٦	гwa	o's	-co	MPL	.EM	EN	Г			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	
Augend Register	0	0	1	0	1	1	1	1		z	
Addend Register	0	1	0	0	1	1	1	0		Ν	
Sum Register	0	1	1	1	1	1	0	1		۷	
-		1	1	1	1	1	0	1		V	

3.	Determine	the	values	of	the	status	bits.

Carry-In Bits         0         0         0         1         1         1         0         0         C         0           Augend Register         0         0         1         0         1         1         1         1         Z         0           Addend Register         0         1         0         1         1         1         1         Z         0           Sum Register         0         1         1         1         1         0         N         0		Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Addend Register         0         1         0         1         1         1         0         N         0	Carry-In Bits	0	0	0	1	1	1	0	0		С	0
	Augend Register	0	0	1	0	1	1	1	1		z	0
Sum Register 0 1 1 1 1 1 0 1 V 0	Addend Register	0	1	0	0	1	1	1	0		N	0
	Sum Register	0	1	1	1	1	1	0	1		V	0

	٦	ΓWC	)'S	-CO	MPI	.EM	EN	Г			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	0
Augend Register	0	0	1	0	1	1	1	1	+47	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	0
Sum Register	0	1	1	1	1	1	0	1	+125	v	0
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# 1. Set up the problem.

0			-			2	1	Value	Bits
0									С
	0	1	0	1	1	1	1		z
0	1	0	0	1	1	1	0		N
									V

	5	SIG	NEC	)-M	AGI	VIT	UDE	-		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	x	0	0	1	1	1	0	0	· ulde	C
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		V
21-Apr-2005				2005 <i>C</i> I	harles /	Abzug			57	

3. Det	erm	ine	the	val	ues	of	the	sta	tus bit:	5.	
	5	SIG	NEC	)-M	AGI	VIT	UDE	3			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	х	0	0	1	1	1	0	0		С	0
Augend Register	0	0	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	0
Sum Register	0	1	1	1	1	1	0	1		v	0
Sum Register	0	1	1	1	1	1	0	1	<u> </u>	<b>V</b>	0
21-Apr-2005			0 ;	2005 C	harles i	Abzug			58		

	5	SIG	NEC	)-M	AGI	VIT	UDE				
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	×	0	0	1	1	1	0	0		C	0
Augend Register	0	0	1	0	1	1	1	1	+47	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	0
Sum Register	0	1	1	1	1	1	0	1	+125	V	0
	1								I		

	SAT	UR	ATI	ON	AR	ITŀ	IWE	TIC		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu Bits
Carry-In Bits										С
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register										V
				2005 0	harles /				60	

						TIL	1/1/1	TIC	•	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		V

	SAI	UR	ATI	ON	AR	ITH	IWE	TIC		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С
Augend Register	0	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		v

	SAT	UR	ATI	ON	AR	ITH	IWE	TIC		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С
Augend Register	0	0	1	0	1	1	1	1	(+)47	z
Addend Register	0	1	0	0	1	1	1	0	(+)78	N
Sum Register	0	1	1	1	1	1	0	1	(+)125	v
21-Apr-2005			0	2005 <i>C</i> I	narles /	Abzug			63	

	SEC	ON	DA	uge	nd-	Add	lend	Pa	ir	
Augend Register	0	1	1	0	1	1	1	1		1
Addend Register	0	1	0	0	1	1	1	0		
Sum Register										
21-Apr-2005			0 ;	2005 CI	narles /	Abzug			64	

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits										С	-
Augend Register	0	1	1	0	1	1	1	1		z	
Addend Register	0	1	0	0	1	1	1	0		Ν	
Sum Register										۷	
-					-	_	-				

"UNSIGN		<u> </u>	-	· ·	_	•	-	-		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С
Augend Register	0	1	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	0	1	1	1	1	0	1		v

# 2. Carry out the operation.

"UNSIGN	ED"	(N	on-l	Expl	licit	ly-S	bign	ed)	INTEG	ER	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	1
Sum Register	1	0	1	1	1	1	0	1		v	0
21-Apr-2005			6	2005 C	harles	Abzug			67		

4.	Determine	decimal	values	of	register	contents.
----	-----------	---------	--------	----	----------	-----------

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	-	tatus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1	(+)111	z	0
Addend Register	0	1	0	0	1	1	1	0	(+)78	Ν	1
Sum Register	1	0	1	1	1	1	0	1	(+)189	V	0

	(	ONE	s'-	co	MPL	EM	ENT	-		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu: Bits
Carry-In Bits										C
Augend Register	0	1	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register										V
21-Apr-2005			6	2005 C	harles	Abzug			69	

	2.	Ca	rry	out	the	op	erat	tion.		
		ON	ES'	CON	NPLI	EME	INT			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С
Augend Register	0	1	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	0	1	1	1	1	0	1		V
21-Apr-2005			0	2005 <i>C</i> I	harles /	Abzug			70	

Bit 8		Bit								
	7	6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits 1	0	0	1	1	1	0	0		C	0
Augend Register 0	1	1	0	1	1	1	1		z	0
Addend Register 0	1	0	0	1	1	1	0		Ν	1
Sum Register 1	0	1	1	1	1	0	1		V	1
Determina C	tion ( riteri							plement:		

	Bit 8	Bit	Bit	Bit	Bit	Bit 3	Bit 2	Bit	Decimal		atus
	•	7	6	5	4	•	-	1	Value	-	its
Carry-In Bits	1	0	0	1	1	1	0	0		C	0
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	1
Sum Register	1	0	1	1	1	1	0	1		V	1
Detern		ion c iteri							plement:		
Human Criterio	on: A	ugenc	1 & A	ddend	l have	iden	tical :	sign, i	Sum has op	posi	te si

	(	ONE	s'-	-CO	MPL	EM	ENI	Г			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	1
Sum Register	1	0	1	1	1	1	0	1		V	1
Detern Human Criterio	Cr	iteri	a fo	r Se	tting	the	V	Bit	plement: Sum has ar	nos	te si

	Bit	Decimal	St	atus							
	8	7	6	5	4	3	2	1	Value		Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	1
Sum Register	1	0	1	1	1	1	0	1		V	1
OTE, since the 'V the <i>correct</i> su								e Sur	n Register	is t	he ∧

	(	ONE	:s'-	CO	MPL	EMI	ENT	•			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		C	0
Augend Register	0	1	1	0	1	1	1	1	+111	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	1
Sum Register	1	0	1	1	1	1	0	1	-66	v	1

		5.	-co	MPL	.EM	EN	Г			
Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
									С	
0	1	1	0	1	1	1	1		z	
0	1	0	0	1	1	1	0		Ν	
									۷	
	8	8 7 0 1	8 7 6 0 1 1	8         7         6         5           0         1         1         0	8         7         6         5         4           0         1         1         0         1	8         7         6         5         4         3           0         1         1         0         1         1	8         7         6         5         4         3         2           0         1         1         0         1         1         1	8         7         6         5         4         3         2         1           0         1         1         0         1         1         1         1	8         7         6         5         4         3         2         1         Value           0         1         1         0         1         1         1         1         1	8         7         6         5         4         3         2         1         Value

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Sta Bi
Carry-In Bits	1	0	0	1	1	1	0	0		C
Augend Register	0	1	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		Ν
Sum Register	1	0	1	1	1	1	0	1		V

			)'S					-			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		N	1
Sum Register	1	0	1	1	1	1	0	1		V	1
Deterr			of O a fo						plement:		

Bit         Dit         Dit <th></th> <th>٦</th> <th>۲WC</th> <th><b>)'S</b></th> <th>-CO</th> <th>MPL</th> <th>.EM</th> <th>EN</th> <th>Г</th> <th></th> <th></th>		٦	۲WC	<b>)'S</b>	-CO	MPL	.EM	EN	Г		
Augend Register         0         1         0         1         1         1         Z         0           Addend Register         0         1         0         1         1         1         1         Z         0           Addend Register         0         1         0         1         1         1         0         N         1           Sum Register         1         0         1         1         1         0         N         1           Sum Register         1         0         1         1         1         0         1         V         1           Determination of Overflow in Two's-Complement:         Criteria for Setting the         V         Bit										 	
Addend Register 0 1 0 0 1 1 1 1 0 N 1 Sum Register 1 0 1 1 1 1 0 1 V 1 Determination of Overflow in Two's-Complement: Criteria for Setting the V Bit	Carry-In Bits	1	0	0	1	1	1	0	0	С	0
Sum Register 1 0 1 1 1 1 0 1 V 1 Determination of Overflow in Two's-Complement: Criteria for Setting the V Bit	Augend Register	0	1	1	0	1	1	1	1	z	0
Determination of Overflow in Two's-Complement: Criteria for Setting the V Bit	Addend Register	0	1	0	0	1	1	1	0	Ν	1
Criteria for Setting the $V$ Bit	Sum Register	1	0	1	1	1	1	0	1	v	1
		Cr	iteri	a fo	r Se	tting	the	V	Bit	posi	ite si

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1		z	0
	0	1	0	0	1	1	1	0		N	1
Addend Register	U				•	•		-			
Addend Register Sum Register	1	0	1	1	1	1	0	1		V	1

	٦	W	)'s	-co	MPL	.EM	EN	Г			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	1
Sum Register	1	0	1	1	1	1	0	1		V	1
OTE, since the 'V' the <i>correct</i> su								e Sur	n Register	is 1	the A

	Bit	FWC Bit				Bit	Bit	Bit	Decimal	St	atus
	8	7	6	5	4	3	2	1	Value	Bits	
Carry-In Bits	1	0	0	1	1	1	0	0		С	0
Augend Register	0	1	1	0	1	1	1	1	+111	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	N	1
Sum Register	1	0	1	1	1	1	0	1	-67	۷	1

	Bit	Bit	Bit	Bit	Bit		Bit		NG Decimal	<i>c</i> .	tatus
	8 8	7	6 6	5	ыт 4	ыт 3	2	1	Value		ratus Bits
Carry-In Bits										С	
Augend Register	0	1	1	0	1	1	1	1		z	
Addend Register	0	1	0	0	1	1	1	0		Ν	
Sum Register										۷	

SI	GNE	D-1	MAG	<b>NI</b>	TUE	E I	INT	EGE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	х	0	0	1	1	1	0	0		С
Augend Register	0	1	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	0	0	1	1	1	1	0	1		v

SI	GNE	D-1	MAG	<b>SNI</b>	TU	E 1	NT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	×	0	0	1	1	1	0	0		С	1
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	0
Sum Register	0	0	1	1	1	1	0	1		v	1
21-Apr-2005				2005 <i>C</i> I	harles	abzug			85		

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	х	0	0	1	1	1	0	0		С	1
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	0
C Desister	0	0	1	1	1	1	0	1		v	1
Sum Register	U	•	-	-	-	-	-	-		•	-
-	ninat	tion	of O	verf	-	n Si	-	-Ma	gnitude:		_

3. Det	erm	ine	the	val	ues	of	the	sta	tus bit:	5.	
SI	GNE	D-1	MAG	INE	TU	E 1	NT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	х	0	0	1	1	1	0	0		С	1
Augend Register	0	1	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		Ν	0
Sum Register	0	0	1	1	1	1	0	1		۷	1
	Cri	terio	on fo	or Se	ettin	g the	2 V	Bit			
Carry-OUT fr Bit <u>7</u> in thi				-	ant <u>11</u>	AGN	TUDI	E Bit	(MSB), i.e.	., fr	om
21-Apr-2005			0	2005 C	harles /	Abzug			87		

4. Determine decimal values of register contents.

SI	GNE	D-I	MAG	INE	TUE	E I	:NT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	х	0	0	1	1	1	0	0		С	1
Augend Register	0	1	1	0	1	1	1	1	+111	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	0
Sum Register	0	0	1	1	1	1	0	1	+61	۷	1
21-Apr-2005				2005 <i>C</i> I	narles /	Abzug			88		

	8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	3	<u> </u>	0	5	-	3	2	1	value	С	DIIS
Augend Register	0	1	1	0	1	1	1	1		z	
	0	1	0	0	1	1	1	0		N	
Addend Register Sum Register	0	1	0	0	1	1	1	0		V	

		AII		AR	115		ITC	•	
Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
1	0	0	1	1	1	0	0		С
0	1	1	0	1	1	1	1		z
0	1	0	0	1	1	1	0		N
1	0	1	1	1	1	0	1		v
	8 1 0 0	8         7           1         0           0         1           0         1	8         7         6           1         0         0           0         1         1           0         1         0	8         7         6         5           1         0         0         1           0         1         1         0           0         1         0         0	8         7         6         5         4           1         0         0         1         1           0         1         1         0         1           0         1         1         0         1           0         1         0         0         1	8         7         6         5         4         3           1         0         0         1         1         1           0         1         1         0         1         1         1           0         1         1         0         1         1         1           0         1         0         0         1         1         1	8         7         6         5         4         3         2           1         0         0         1         1         1         0           0         1         1         1         1         0           0         1         1         0         1         1         1           0         1         0         0         1         1         1         1	8         7         6         5         4         3         2         1           1         0         0         1         1         1         0         0           0         1         1         1         1         0         0           0         1         1         0         1         1         1         1           0         1         0         0         1         1         1         1	8         7         6         5         4         3         2         1         Value           1         0         0         1         1         1         0         0           0         1         1         1         1         0         0         -           0         1         1         1         1         1         1         -           0         1         1         1         1         1         1         -

	SAT	UR	ATI	ON	AR	IT۲	IWE	TIC	:	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		C
Augend Register	0	1	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	0	1	1	1	1	0	1		v
Sum Register	1	0	1	1	1	1	0	1		V

	SAT	UR	ATI	:ON	AR	ITH	IWE	TIC	:	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С
Augend Register	0	1	1	0	1	1	1	1	+111	z
Addend Register	0	1	0	0	1	1	1	0	+78	N
Sum Register	1	0	1	1	1	1	0	1	+189	v

	тн	IIRC	Αι	ıgen	id-A	\dde	end	Pair			
Augend Register	1	0	1	0	1	1	1	1		٦	
Addend Register	0	1	0	0	1	1	1	0			
Sum Register											
21-Apr-2005			0	2005 <i>C</i> I	harles /	Abzug			9	93	

			Set								
UNSIGN		-			-		_			S	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits										С	
Augend Register	1	0	1	0	1	1	1	1		z	
Addend Register	0	1	0	0	1	1	1	0		Ν	
Sum Register										۷	
Addend Register		-	-	-	-	-	-	-		N	
			_								
21-Apr-2005				2005 C	harles /	Abzug			94		

	2.	Ca	rry	out	the	e op	erat	tion		
UNSIGN	IED	(No	on-E	Expl	icitl	y-S	igne	ed)	Number	s
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	1		C
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	0	1		v
Juni Register	1	1	1	1	1	1	0	1	<u> </u>	<u> </u>
21-Apr-2005			•	2005 <i>C</i> I	harles /	Abzug			95	

UNSIGN	1ED	(No	on-E	Expl	icitl	y-S	igne	2d)	Number	s	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	1		C	0
Augend Register	1	0	1	0	1	1	1	1		z	0
Addend Register	0	1	0	0	1	1	1	0		N	0
Sum Register	1	1	1	1	1	1	0	1		V	0
21-Apr-2005				2005 C	harles /	abzug			96		

UNSIGN	1ED	(No	on-E	xpl	icitl	y-S	igne	2d)	Number	S	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	1		С	0
Augend Register	1	0	1	0	1	1	1	1	(+)175	z	0
Addend Register	0	1	0	0	1	1	1	0	(+)78	Ν	0
Sum Register	1	1	1	1	1	1	0	1	(+)253	v	0
21-Apr-2005				2005 C	harles /	Abzua			97		

# 1. Set up the problem. Image: constraint of the set of t

NO	Bit 8	- <i>C</i> (Bit	OMF Bit 6					EGE Bit	RS Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	1		C
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	0	1		v
21-Apr-2005				2005 <i>C</i> I		4 h m			99	

Addend Register         0         1         0         0         1         1         1         0         N         1           Sum Register         1         1         1         1         1         0         1         V         0	10	IES	'-C	OWE	LEA	VEV	IT I	NT	EGE	RS		
Augend Register         1         0         1         0         1         1         1         1         Z         0           Addend Register         0         1         0         1         1         1         1         Z         0           Addend Register         0         1         0         1         1         1         0         N         1           Sum Register         1         1         1         1         0         1         V         0												
Addend Register       0       1       0       0       1       1       0       N       1         Sum Register       1       1       1       1       1       0       1       1       1         OTE that BOTH the 'C' bit       AND the 'V' bit are 0s. Therefore, the content of the the theorem       1	Carry-In Bits	0	0	0	1	1	1	0	1		С	0
Sum Register 1 1 1 1 1 1 0 1 $V$ 0	Augend Register	1	0	1	0	1	1	1	1		z	0
OTE that <u>BOTH</u> the 'C' bit <u>AND</u> the 'V' bit are 0s. Therefore, the content of	Addend Register	0	1	0	0	1	1	1	0		Ν	1
	Sum Register	1	1	1	1	1	1	0	1		V	0
								0-	These	fono the		ent (
											con	

	1E2	CC	OWP	LE/	NEN	IT I	NT.	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	1		С	0
Augend Register	1	0	1	0	1	1	1	1	-80	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	1
Sum Register	1	1	1	1	1	1	0	1	-2	v	0
21-Apr-2005				200E C	harles /				101		

TW	10's	-		-						
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	State Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register										V

TW	0'									
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu Bits
Carry-In Bits	0	0	0	1	1	1	0	1		С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	0	1		V
					harles /				103	

3.	Determine	the	values	of	the	status	bits.

Carry-In Bits         0         0         0         1         1         1         0         1         C           Augend Register         1         0         1         0         1         1         1         1         1         Z           Addend Register         0         1         0         1         1         1         1         0         N           Sum Register         1         1         1         1         1         1         0         1         V		Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Addend Register         0         1         0         1         1         1         0         N	Carry-In Bits	0	0	0	1	1	1	0	1		С	0
	Augend Register	1	0	1	0	1	1	1	1		z	0
Sum Register 1 1 1 1 1 1 0 1 V	Addend Register	0	1	0	0	1	1	1	0		N	1
	Sum Register	1	1	1	1	1	1	0	1		V	0

ТМ	0'	5-C	OMI	PLE	MEN	IL I	INT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	0	0	0	1	1	1	0	1		С	0
Augend Register	1	0	1	0	1	1	1	1	-81	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	1
Sum Register	1	1	1	1	1	1	0	1	-3	۷	0
21-Apr-2005				2005 <i>C</i> I	harles /	Abzug			105		

SI	GNE		Set MAG	ÎNI	TUL	•	NT	EGE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register										v
Sum Register										V
21-Apr-2005			0;	2005 <i>C</i>	harles /	Abzug			106	

SI	GNE	D-1	MAG	INE	TUD	E 1	INT	EGE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1	-47	z
Addend Register	0	1	0	0	1	1	1	0	+78	N
Sum Register									+31	V

The problem requires the addition of numbers of opposite sign.

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ALGORITHM for ADDIT SIGN:	ION of SIGNED-MAGNITUDE	NUMBERS of OPPOSITE
<ol> <li>Replicate its sign bit i</li> <li>Subtract the MAGN magnitude of the L</li> </ol>	er (Augend or Addend) has the L. n the SUM REGISTER. NITUDE of the SMALLER-MAGH ARGER-MAGNITUDE number. NE FIELD of the SUM REGISTER	NITUDE number from the
21-Apr-2005	© 2005 Charles Abzug	108

Bit Bi 8 7	Bit 6	Bit 5	SIGNED-MAGNITUDE INTEGERS Bit Bit Bit Bit Bit Bit Bit Bit Decimal Status											
		5	4	3	2	1	Value		tatus Bits					
								С						
1 0	1	0	1	1	1	1	-47	z						
0 1	0	0	1	1	1	0	+78	Ν						
0 0	0	1	1	1	1	1	+31	v						
(	0 1	0 1 0	0 1 0 0	0 1 0 0 1	0 1 0 0 1 1	0 1 0 0 1 1 1	0 1 0 0 1 1 1 0	0 1 0 0 1 1 1 0 +78	0 1 0 0 1 1 1 0 +78 N					

4 7 91	Bit 8	Bit	D:+						RS		
4 7 8.1	0	7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	0	0	0	1	1	1	0	1		С	0
Augend Register	1	0	1	0	1	1	1	1	-80	z	0
Addend Register	0	1	0	0	1	1	1	0	+78	Ν	1
Sum Register	1	1	1	1	1	1	0	1	-3	v	0

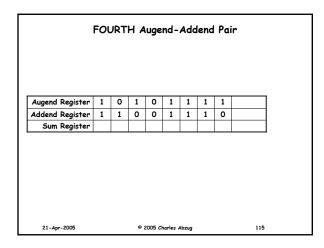
Г

	1 SAT			up ON		·			:	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register										v
	0	1	0	0	1	1	1	0		
21-Apr-2005			0;	2005 <i>C</i> I	harles a	Abzug			111	

	2.	Ca	rry	out	the	ор	erat	ion.		
	SAT	UR	ATI	ON	AR	ITH	IWE	TIC	:	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	1		С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	0	1		V
21-Apr-2005			0	2005 <i>C</i> I	narles A	lbzug			112	

3. Saturatio	on A	rith	imet	tic:	Do	es i	NO	T us	e Statı	ıs bits
	SAT	UR	ATI	:ON	AR	ITH	IME	TIC	:	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	1		C
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	0	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	0	1		V
Addend Register	0	1	0	0	1	1	1	0		N
21-Apr-2005			0	2005 C	harles /	Abzug			113	

	SAT	UR	ATI	ON	AR	ITH	IWE	TIC		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	1		С
Augend Register	1	0	1	0	1	1	1	1	(+)175	z
Addend Register	0	1	0	0	1	1	1	0	(+)78	N
Sum Register	1	1	1	1	1	1	0	1	(+)253	v



UNSIGNE	ED (	"No	n-E	xpli	citly	/-5	igne	1 (b	UMBE	RS
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register										v

	2.	Ca	rry	out	the	ор	erat	tion		
UNSIGNE	D (	"No	n-E	xpli	citly	/-S	igne	d) 1	UMBE	RS
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	0		C
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		v
21-Apr-2005			0	2005 C	harles i	Abzug			117	

it   3	Bit	Bit 6	Bit 5	Bit 4	Bit 3	<u> </u>	<u> </u>	<b>Decimal</b>	St	atus Bits
> >		-	-	•	-	-	-	value	_	1
, i	0	1	0	1	1	1	1		z	0
1	1	0	0	1	1	1	0		N	0
5	1	1	1	1	1	0	1		۷	1
	)	0 0 0 1	0 0 0 0 1 1 0	0         0         1           0         1         0           1         0         0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	0         0         0         1         1         1         0           0         1         0         1         1         1         0           0         1         0         1         1         1         1           1         0         0         1         1         1         1	0         0         1         1         0         0           0         1         0         1         1         1         0         0           0         1         0         1         1         1         1         1         1           1         0         0         1         1         1         1         0	0         0         1         1         1         0         0           0         1         1         1         0         0         1         1         1         1           1         0         0         1         1         1         1         0	0         0         1         1         1         0         0         C           0         1         1         1         0         0         C           0         1         0         1         1         1         1         Z           1         0         0         1         1         1         0         N

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	1
Augend Register	1	0	1	0	1	1	1	1	(+)175	z	0
Addend Register	1	1	0	0	1	1	1	0	(+)206	Ν	0
Sum Register	0	1	1	1	1	1	0	1	(+)125	v	1
21-Apr-2005			6	2005 C	harles	abzua			119		

ON	IES	'-C	OMF	LEN	VEN	ті	NT	EGE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register										v
	<u> </u>	1	1	1	<u> </u>	<u> </u>				
21-Apr-2005			0	2005 <i>C</i> I	norles	have			120	

ON	IES	'-C(	OWb	'LE/	VEV	IT I	NT	EGE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	0		C
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		v

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	1
Augend Register	1	0	1	0	1	1	1	1		z	0
Addend Register	1	1	0	0	1	1	1	0		Ν	0
Sum Register	0	1	1	1	1	1	0	1		V	1

ON	IES	'-C	OWb	LEN	NEN	IT I	NT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	1
Augend Register	1	0	1	0	1	1	1	1	-80	z	0
Addend Register	1	1	0	0	1	1	1	0	-49	Ν	0
Sum Register	0	1	1	1	1	1	0	1	+125	v	1
					1						

	1	ι. :	Set	up	the	pro	bler	n.		
TW	0':	5-C	OMI	PLE	NEN	IT I	INT	EGE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register										V
21-Apr-2005				2005 <i>C</i> I	narles /	Abzug			124	

ТИ	/0'\$	5-C	OMI	PLE/	MEN	1T ]	INT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	
Augend Register	1	0	1	0	1	1	1	1		z	
Addend Register	1	1	0	0	1	1	1	0		Ν	
Sum Register	0	1	1	1	1	1	0	1		۷	
Addend Register	1	-	-	-	-	-	-	-			

ти	0':	5-C	OMI	PLE	MEN	1T ]	INT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	1
Augend Register	1	0	1	0	1	1	1	1		z	0
Addend Register	1	1	0	0	1	1	1	0		N	0
Sum Register	0	1	1	1	1	1	0	1		v	1

# 3 Determine the values of the status bits

L

ТМ	10's	5-C	OMI	PLE	MEN	<u>т</u> т	INT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С	1
Augend Register	1	0	1	0	1	1	1	1	-81	z	0
Addend Register	1	1	0	0	1	1	1	0	-50	Ν	0
Sum Register	0	1	1	1	1	1	0	1	+125	۷	1
-	-	-	-	-	-	-	-	-			-
21-Apr-2005			0	2005 <i>C</i> I	harles /	Abzug			127		

# 1. Set up the problem.

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register										V

SI	GNE	D-1	MAG	INE	TUD	E 1	INT	EGE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu: Bits
Carry-In Bits	х	0	0	1	1	1	0	0		C
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	0	1		V
21-Apr-2005				2005 <i>C</i> I	harles	Abzug			129	

SI	SNE	D-1	MAG		TUE	DE I	NT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		ratus Bits
Carry-In Bits	х	0	0	1	1	1	0	0		С	0
Augend Register	1	0	1	0	1	1	1	1		z	0
Addend Register	1	1	0	0	1	1	1	0		Ν	1
Sum Register	1	1	1	1	1	1	0	1		۷	0
21-Apr-2005				2005 <i>C</i> I	narles /	Abzug			130		

SI	GNE	D-I	MAG	<b>NI</b>	TUD	ΕI	NT	EGE	RS		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	x	0	0	1	1	1	0	0		С	0
Augend Register	1	0	1	0	1	1	1	1	-47	z	0
Addend Register	1	1	0	0	1	1	1	0	-78	Ν	1
Sum Register	1	1	1	1	1	1	0	1	-125	v	0
21-Apr-2005			0	2005 CI	harles /	Abzua			131		

Bit 8	Bit		0:4	Bit	Bit	D:4	Dit	Desimal	Chatura
	7	Bit 6	Bit 5	8it 4	3	Bit 2	Bit 1	Decimal Value	Status Bits
									С
1	0	1	0	1	1	1	1		z
1	1	0	0	1	1	1	0		N
									v
	-								

	SAT	UR.	ATI	:ON	AR	ITH	IWE	тіс		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	0	1	1	1	1	1	0	1		V

	SAT	UR	ATI	ON	AR	ITh	IWE	TIC		_
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	0		С
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	1	1		v

3. Saturatio	on A	rith	imet	tic:	Do	es i	NO	T us	e Statu	ıs bits
	SAT	UR	ATI	:ON	AR	ITH	IME	TIC	:	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	0	0	0	1	1	1	0	0		C
Augend Register	1	0	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	1	1		v
<i>HOWEVER, in pla</i> "Unsigned-Numb via hardware to Explicitly-Signe	oer" o the	arith : <u>SA</u>	metio TURA	c, th ATIO	e co <u>N</u> le	ntent vel:	· of the	the large	Sum Regi: st "Unsigi	ster is s ned" (No
21-Apr-2005			0	2005 C	harles d	Abzug			135	

Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
0	0	0	1	1	1	0	0		С
1	0	1	0	1	1	1	1	(+)175	z
1	1	0	0	1	1	1	0	(+)206	N
1	1	1	1	1	1	1	1	(+)255	v
	0 1 1	0 0 1 0 1 1	0         0         0           1         0         1           1         1         0	$\begin{array}{c ccccc} 0 & 0 & 0 & 1 \\ \hline 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \end{array}$	0         0         0         1         1           1         0         1         0         1         1           1         1         0         0         1         1	0         0         0         1         1         1           1         0         1         0         1         1         1           1         1         0         0         1         1         1           1         1         0         0         1         1         1	0         0         0         1         1         1         0           1         0         1         0         1         1         1         1           1         1         0         1         1         1         1         1           1         1         0         0         1         1         1         1	0         0         0         1         1         1         0         0           1         0         1         1         1         0         0         1         0         1         1         1         0         1         1         1         0         1         1         1         0         1         1         1         0         1         1         1         0         1         1         1         0         1         1         0         1         1         1         0         1         1         1         0         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1	0         0         0         1         1         0         0           1         0         1         1         1         0         0           1         0         1         1         1         1         (+)175           1         1         0         1         1         1         0         (+)206

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SUBTRA				n So the				rith	metic		
S	4TU	RA	гіо	N A	RI	۲H۸	NET:	IC			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus its
										С	
Minuend Register	1	0	1	0	1	1	1	1		z	
Subtrahend Register	1	1	0	0	1	1	1	0		N	
Difference Register										v	
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SUBTRA 2.				n So t th					metic		
				N A							
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus its
										С	
Minuend Register	1	0	1	0	1	1	1	1		z	
Subtrahend Register	1	1	0	0	1	1	1	0		Ν	
Difference Register	0	0	0	0	0	0	0	0		۷	
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## 4. Determine decimal values of register contents.

3. Saturation			etic:						Status	bits	5.
	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit			atus
	8	7	6	5	4	3	2	1	Value	В	its
										С	
Minuend Register	1	0	1	0	1	1	1	1		z	
Subtrahend Register	1	1	0	0	1	1	1	0		Ν	
Difference Register	0	0	0	0	0	0	0	0		V	
21-Apr-2005			₽ 2005	Charles	Abzua				139		

3. Saturation	Arit	hme	etic	D	oes	NC	7 <i>T</i> u	se S	Status	bits	5.
Si	4TU	RA	TIO	N A	RI	ΓHN	NET:	IC			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus its
										С	
Minuend Register	1	0	1	0	1	1	1	1		z	
Subtrahend Register	1	1	0	0	1	1	1	0		Ν	
Difference Register	0	0	0	0	0	0	0	0		v	
In ordinary "Unsigne subtracted from a "Unsigned Numbers positive), and the <i>HOWEVER</i> , under <i>underflow</i> , the cc adjusted via the p smallest "Unsigned 21-Apr-2005	noth " ar refor the nten roce:	er, s e ne rules t of ssor's per"	small cesso ne tr of the s ha	er nu rily Satu Dif dwar the i	umber non- differ ratio fere re to regis	r, ai nega rence n Ar nce the ter c	n <i>un</i> tive car ithm Regi: <u>SA</u> 1	derfla (i.e. not etic, ster <u>FURA</u>	ow occurs , either : be repre <i>instead</i> is autom <u>TION</u> lev	s, s zero sent of natic vel:	ince or ted. <i>the</i> ally the

SUBTRACTION in Saturation Arithmetic

Si			TIO					_			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus its
										С	
Minuend Register	1	0	1	0	1	1	1	1	(+)175	z	
Subtrahend Register	1	1	0	0	1	1	1	0	(+)206	Ν	
Difference Register	0	0	0	0	0	0	0	0	0	V	
NOTE that by the	e ri	les	of	Sa	ture	atio	n A	ritk	imetic,		5

	FI	FTH	ł Au	ıgen	d-A	dde	nd	Pair		
Augend Register	1	1	1	0	1	1	1	1		1
Addend Register	1	1	0	0	1	1	1	0		1
Sum Register										]
21-Apr-2005			0;	2005 <i>C</i> I	narles /	Abzug			142	

UNSIGNE	Bit	Bit	Bit	Bit	Bit	Bit	<u> </u>	-	Decimal	r –	tatus
	8	7	6	5	4	3	2	1	Value		Bits
Carry-In Bits										С	
Augend Register	1	1	1	0	1	1	1	1		z	
Addend Register	1	1	0	0	1	1	1	0		Ν	
Sum Register										۷	
-	1	1	0	0	1	1	1	0			

UNSIGNE	D (	"No	n-E	xpli	citly	y-S	igne	d) 1	NUMBE	RS
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С
Augend Register	1	1	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	1	0	1	1	1	1	0	1		V
21-Apr-2005				2005 C	harles /				144	

UNSIGNE	ED (	"No	n-E	xpli	citly	y-S	igne	1 (b	NUMBE	RS	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits	1	0	0	1	1	1	0	0		C	1
Augend Register	1	1	1	0	1	1	1	1		z	0
Addend Register	1	1	0	0	1	1	1	0		Ν	0
Sum Register	1	0	1	1	1	1	0	1		v	1
21-Apr-2005			6	2005 <i>C</i> I	harles /	Abzua			145		

4. C	Determine	decimal	values	of	register	contents.
------	-----------	---------	--------	----	----------	-----------

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	1
Augend Register	1	1	1	0	1	1	1	1	(+)239	z	0
Addend Register	1	1	0	0	1	1	1	0	(+)206	Ν	0
Sum Register	1	0	1	1	1	1	0	1	(+)189	V	1

				•		pro				
		ONE	s'-	-co	MPL	.EM	ENT	Г		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										C
Augend Register	1	1	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register										v
21-Apr-2005			0	2005 <i>C</i> I	harles a	Abzug			147	

		Ca ONE									
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	
Augend Register	1	1	1	0	1	1	1	1		z	
Addend Register	1	1	0	0	1	1	1	0		Ν	
Sum Register	1	0	1	1	1	1	0	1		۷	
						<u>.</u>					
21-Apr-2005				2005 <i>C</i>	harles /	Abzug			148		

		ONE	s'-	co	MPL	EM.	ENT	-			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits	1	0	0	1	1	1	0	0		C	1
Augend Register	1	1	1	0	1	1	1	1		z	0
Addend Register	1	1	0	0	1	1	1	0		Ν	1
Sum Register	1	0	1	1	1	1	0	1		V	0
Sum Register	1	0	1	1	1	1	0	1	efore, it is	V	0

	0	DNE	s'-	col	NPLI	eme	NT				
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits	0	0	0	0	0	0	1	1		С	0
Prior Content of										z	0
Sum Register:	1	0	1	1	1	1	0	1		Ν	1
New Sum Register	1	0	1	1	1	1	1	0		۷	0
NOTE that the 'C' bi									ore, it is r n Register		

	0	ONE	s'-	-CO	MPL	EM	ENT	•			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	0	0	0	0	0	0	1	1		С	0
Augend Register	1	1	1	0	1	1	1	1	-16	z	0
Addend Register	1	1	0	0	1	1	1	0	-49	Ν	1
Sum Register	1	0	1	1	1	1	1	0	-65	v	0
21-Apr-2005			0	2005 <i>C</i> I	harles	Abzuo			151		

# 1. Set up the problem.

	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Statu Bits
Carry-In Bits										С
Augend Register	1	1	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register										V

						e op		tion.		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		C
Augend Register	1	1	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	1	0	1	1	1	1	0	1		v
21-Apr-2005			0	2005 C	harles /	Abzug			153	

	٦	rwa	o's	-CO	MPL	.EM	EN	Г			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		ratus Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С	1
Augend Register	1	1	1	0	1	1	1	1		z	0
Addend Register	1	1	0	0	1	1	1	0		N	0
Sum Register	1	0	1	1	1	1	0	1		v	0
n TWO'S COMPLI <u>ignore</u> the 'C' b precision addition.	it.										

cimal Status					WILL L	-20	1.2	гwс	1	
alue Bits	Decimal Value	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	
C 1		0	0	1	1	1	0	0	1	Carry-In Bits
-17 Z 0	-17	1	1	1	1	0	1	1	1	Augend Register
-50 N 1	-50	0	1	1	1	0	0	1	1	Addend Register
-67 V 0	-67	1	0	1	1	1	1	0	1	Sum Register
-50 N	-50	0	1	1	1	0	0	1	1	Addend Register

		SIG	NEC	)-M	AGI	<b>JIT</b>	UDE	3		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits										С
Augend Register	1	1	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register										v
					harles /				156	

		20		)-M	AGI	AT I	UD	-		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	x	0	0	1	1	1	0	0		C
Augend Register	1	1	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	1	0	1	1	1	1	0	1		v

	5	SIG	NEC	)-M	AGI	JIT	UDE	2			
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus Bits
Carry-In Bits	х	0	0	1	1	1	0	0		С	1
Augend Register	1	1	1	0	1	1	1	1		z	0
Addend Register	1	1	0	0	1	1	1	0		Ν	1
Sum Register	1	0	1	1	1	1	0	1		v	1

Г

SIGNED-MAGNITUDE											
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits	x	0	0	1	1	1	0	0		C	1
Augend Register	1	1	1	0	1	1	1	1	-111	z	0
Addend Register	1	1	0	0	1	1	1	0	-78	Ν	1
Sum Register	1	0	1	1	1	1	0	1	-61	v	1
Sum Register	1	0	1	1	1	1	0	1	-61	<b>v</b>	1

1. Set up the problem.											
	Bit 8	Bit 7	Bit 6	Bit 5	AR Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		tatus Bits
Carry-In Bits										С	
Augend Register	1	1	1	0	1	1	1	1		z	
Addend Register	1	1	0	0	1	1	1	0		Ν	
Sum Register										۷	
21-Apr-2005			0 ;	2005 <i>C</i> I	harles /	Abzug			160		

SATURATION ARITHMETIC											
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value		atus lits
Carry-In Bits	1	0	0	1	1	1	0	0		C	
Augend Register	1	1	1	0	1	1	1	1		z	
Addend Register	1	1	0	0	1	1	1	0		N	
Sum Register	1	0	1	1	1	1	0	1		V	
Addend Register	1	1	0	0	1	1	1	0		N	

	SAT	UR	ATI	ON	AR	ITH	IWE	TIC		
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С
Augend Register	1	1	1	0	1	1	1	1		z
Addend Register	1	1	0	0	1	1	1	0		N
Sum Register	1	1	1	1	1	1	1	1		V
<i>HOWEVER, I</i> occurred in the content the <u>SATUR</u> signed numb	of of	rdin the [ON	ary Sui <u>1</u> le	"U n Ro vel:	nsig egis th	ned ter e l	-Nu is s arge	mbe et v est	er" ari via haro non-e>	thmeti dware «plicitl

SATURATION ARITHMETIC									:	
	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Decimal Value	Status Bits
Carry-In Bits	1	0	0	1	1	1	0	0		С
Augend Register	1	1	1	0	1	1	1	1	+239	z
Addend Register	1	1	0	0	1	1	1	0	+206	N
Sum Register	1	1	1	1	1	1	1	1	+255	V
		o the	e rule	es of	8-	bit	Sat	urat	ion Ari	thmet

Representation of Floating-Point Numbers
Modern physics, chemistry, biology, astronomy, meteorology, and also various disciplines of engineering require the recording of both very large numbers and very small numbers, as well as the performance of mathematical operations upon them.
For such numbers, integer or fixed-point notation is extremely inefficient, since a substantial part of such a representation would have to be taken up with large numbers of leading or trailing zeroes.
For example, the star system Alpha Centauri, the nearest star system from our sun, is <i>approximately</i> 41,153,298,540,000,000 meters away from Earth. The wavelength of Copper K-alpha radiation (a particular type of X-ray used by chemists to measure the dimensions of molecular crystals) is .000000001541 meters.
(continued)

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 Representation of Floating-Point Numbers

 (continued)

 Scientists developed a notational system for the purpose of writing very large and very small numbers without having to use a large number of zeroes. This is called Scientific Notation.

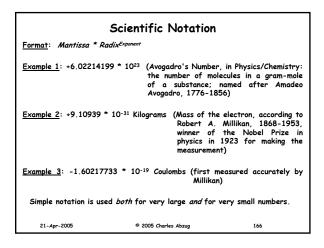
 Computer science makes use of several varieties of notation, all based upon scientific notation, but especially adapted to use in digital computers. These consist of several varieties of a scheme known as Floating-Point Number Representation.

 Scientific Notation is informal, flexible, and highly adaptable.

 Floating-Point Number Representation must necessarily be very carefully defined and specified in each place where it is used, so that programs making use of it will generate results that are correct.

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s	cientific Notation (contin	nued)
5.00 * 10º	$= 0.5 * 10^{1} = 0.05 * 10^{2}$	= 5,000 * 10-3
ONE signific	ns are legal, but the <i>de facto</i> s ant decimal digit (i.e., a digit he mantissa's decimal point.	
(1) Ma (2) Sig (3) Rac (4) Sig	a number represented in Scientif ntissa n of the Mantissa dix (almost always 10 in Scientif n of the Exponent gnitude of the Exponent	
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	Floating-Point F IEEE Star	•	on:
FOUR com	nponents of a number in Float	ing-Point Represent	ation:
	•	EXPLICIT	
(2)	Magnitude of the Mantissa:	EXPLICIT	
(3)	Radix:	IMPLICIT	
(4)	Exponent:	EXPLICIT	
FWO diff	erent levels of precision: SI	NGLE (32-bit) & Do	OUBLE (64-bit)
TWO diff	erent levels of precision: SI (conti		OUBLE (64-bit)

e-Precision: 3-bit Exponent	23-bit Normalized Fractional Significand
Excess-127	Integer bit elided
)	
ble-Precision: <i>Hig</i>	
e-Precision: <i>Hig</i> 11-bit Exponent Excess-1023	

	F	Floating-Point Represent IEEE Standard 754	
1.	Sign bit S	: Sign of the Mantissa = $(-1)^{s}$	
2.	Radix = 2	(NOTE, however, that non-IEEE for numbers have been implemented on radices of 2, 8, and 16.)	
3.	With limi <sup>.</sup>	ted exceptions, Floating Point nur normalized numbers, that is, the e that the mantissa has a value gre $1.0_{10}$ and less than $2.0_{10}$ . Al therefore have a mantissa composed of 1, followed by several fractions and 0s as appropriate. The gen mantissa is: $1.f$ , where $f$ sta component.	exponent is adjusted so cater than <u>or equal to</u> a normalized numbers d of a single integer bit al bits consisting of 1s neral form of such a
		(continued)	
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	Floating-Point Representation: IEEE Standard 754
(cont	ued)
4. Since	every normalized mantissa contains an integer bit of 1, it is not necessary to waste one of the precious available bits to represent it explicitly. Instead, the integer bit of 1 is <u>elided</u> (that is, its presence is implied and therefore it is not explicitly represented anywhere in the memory storage location or in the floating-point register. Only the bits of the fractional portion of the mantissa are represented explicitly, and therefore these bits are called the significand and <u>not</u> the mantissa. of the register or memory storage location. Thus, either 24 bits or 53 bits of precision are obtained from only 23 bits or 52 bits of storage space.
	(continued)
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### Floating-Point Representation: IEEE Standard 754

(continued)

- 5. Special cases: Several representations are specially defined as having values that deviate from the normal pattern. These are:
  - a) Zero: Since the standard Floating-Point representation incorporates an elided integer component of 1, a value of zero would not be exactly representable; it would be necessary to approximate zero by using the value of the smallest non-zero value. This would be 1.0 \* 2<sup>-127</sup> for single-precision, or 1.0 \* 2<sup>-1023</sup> for double-precision.

(continued)

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Floating-Point Representation: IEEE Standard 754				
(continued)				
In fac	ct, there are two repre reserved for zero: +0 (sign bit = 1). For both of these all significand bits are zeroes	n bit = 0) and -0 (sign e, all exponent bits <u>and</u>		
b) Denormalized numbers: If <u>only</u> normalized numbers were represented, then single-precision Floating-Point numbers would be limited to a minimum non-zero value of $\pm 1.0 \times 2^{-127}$ , and double-precision to $\pm 1.0 \times 2^{-1023}$ . The representation in the exponent field of all zeroes is also used to enable the extension of floating-point representation to much smaller non-zero values.				
	(continued)			
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Floating-Point Representation: IEEE Standard 754				
(continued)				
	When the exponent field con the significand field represe fractional mantissa. Thus, t values that can be represente $\pm 2^{-149}$ (single-precision) an precision).	nts a non-normalized the minimum non-zero ad are $\pm 2^{-23} + 2^{-126} =$		
<ol> <li>±Infinity: denoted by <u>BOTH</u> all 1s in the exponent field <u>AND</u> all 0s in the significand field.</li> </ol>				
(continued)				
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Floating-Point Representation: IEEE Standard 754			
(continued)			
7. "Not a Number	(NaN)": In certain cases, operation is defined in indeterminate: for examp ±zero by ±zero, or ±infii attempt to subtract infin attempt to subtract infin attempt to multiply ±infinit are all represented by an of all 1s, together with contains at least one 1. T collectively referred to as t	mathematics as being le, an attempt to divide nity by $\pm infinity$ , or an ity from infinity, or an y by $\pm zero$ . These cases exponent field consisting a significand field that hese representations are	
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