CS-350: Topics for Term Papers

NOTE: Two levels of topics are presented here: numbered major topics, and lettered sub-topics. You may select either a numbered topic, and build you paper around a comparison of several of its sub-topics, or you may choose a lettered sub-topic, and discuss only that item. Only *one* student group will be permitted to function within each major topic (*i.e.*, either on the major topic or on one of its sub-topics).

1. System buses
    a. The Original PC Bus, the PC/AT Bus, and the ISA Bus
    b. Marketplace failures: the MCA and EISA Buses
    c. VESA Local Bus (VLB)
    d. PCI Bus
    e. Advanced Graphics Port (AGP)
    f. IEEE 1394 FireWire, and/or the Universal Serial Bus (USB)
    g. Digital Equipment Corporation (DEC) Unibus
    h. Other buses

2. Device Controllers
    a. Serial Port (COM1, COM2) and Parallel Port (LP1, LP2)
    b. Universal Serial Bus (USB)
    c. Integrated Device Electronics (IDE) and Enhanced IDE (EIDE)
    d. Small Computer System Interface (SCSI) in all its multiple manifestations

3. Main-product-line Intel CPUs
    a. 4004 & 8008
    b. 8086/8088, 80186, 80286
    c. 80386SX/DX & 80486SX/DX
    d. Pentium, Pentium with MMX, Pentium Pro, Pentium II, Xeon, & Celeron (“Socket 370”)
    e. Pentium III & Pentium 4
    f. IA-64: Intel Core 2 Duo, Core 2 Quad, Core 2 Extreme, *etc.*

4. Competitor Chips to Intel: AMD
    a. K5, K6, K7 (Athlon “Slot A”, Duron, Sempron)
    b. Athlon 64 (Opteron, Phenom, Turion)

5. Competitor Chips to Intel:
    a. Cyrix
    b. Rise Technology’s mP6
    c. IDT subsidiary Centaur Technology: WinChip C6, WinChip 2,WinChip 2+, WinChip 3
    d. Transmeta’s Crusoe & Efficeon

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6. Special Instructions for Graphics and Multi-Media
    a. Intel's "MMX" and MMX's "Streaming SIMD" extensions
    b. AMD's "3DNow"

7. Non-Intel-8086-family-Processors:
    1. Motorola 6800/68000 series CPU chips, and machine architectures utilizing these processors
    2. PowerPC CPU and companion chips, and machine architecture
    3. SPARC CPU and machine architecture
    4. MIPS CPU and machine architecture
    5. IBM R/S 6000 CPU and machine architecture
    6. SGI R10000 CPU and machine architecture

10. 64-bit processors of the earlier generation:
    a. DEC/Compaq Alpha CPU and machine architecture
    b. Hewlett-Packard's PA-64

11. Chipsets for PCs

12. Mainframe architecture:
    a. IBM Series 360/370/390, Series 3**6,** & IBM Series 3**8**
    b. Univac/Sperry-Rand
    c. Burroughs

13. Minicomputer architecture:
    a. DEC PDP-series through PDP-11 and/or VAX-11
    b. Data General

14. Fault-Tolerant and High-Availability architectures: Tandem/16, Stratus, VAX-cluster, etc.

15. Supercomputer architecture:
    a. CDC 6600 (the first supercomputer, designed by Seymour Cray (had a RISC instruction set, although the term had not yet been invented), CDC 7600, & CDC 8600
    b. CRAY-1, CRAY-2, CRAY-3, Cray XMP, Cray YMP
    c. Thinking Machines
    d. Intel multi-processor arrays

16. Dynamic Random Access Memory (DRAM)
    a. simple DRAM
    b. Fast Page Mode (FPM) DRAM
    c. Extended Data Out (EDO) DRAM
    d. Burst EDO (BEDO) DRAM
    e. Synchronous DRAM (SDRAM)
    f. Rambus DRAM (RDRAM)
    g. Double Data Rate (DDR) SDRAM

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17. Cache Memory (SRAM)
    a. Associative cache
    b. Direct-Mapped cache
    c. Set-Associative Cache
    d. Sector-Mapped Cache
    e. Synchronous or Pipeline-Burst cache
    f. Write-Through vs. Write-Back
    g. Design and Usage considerations for Instruction Cache vs. Data Cache

18. Measurement of Computer Performance

19. Details of the "Boot" sequence for the PC for different operating systems: differences between *DOS, Windows95/98/Millenium* or *XP/Home, Windows NT* or *XP Professional, Vista,,* and *Linux*

20. Floating-Point Representation and Arithmetic

21. "Plug-and-Play" (affectionately referred to by computer professionals as "Plug-and-P**r**ay")

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