Multiple Choice Questions (Curtin-Dieteman-Sanford: AGP):

The AGP slot is designed for what component?

a) Video Cards
b) Sound cards
c) Keyboard connection
d) ethernet connection

Answer: A

What does Intel plan to replace with the PCI-Express?

A.) AGP
B.) PCI
c.) North Bridge/South Bridge
D.) All of the above

Answer: D

What year did Intel first release the AGP slot for use in its own systems?

A.) 1995
B.) 1997
C.) 1998
D.) 2000

Answer: B

(Imbert-Cook-Drayer: Plug and Play):

1.) Plug and Play was first introduced on what operating system?
a.)Windows 98
b.)Windows 3.1
c.)Windows 95
d.)Linux

2.) Which component within the operating system eliminates conflicting resources?
a.)Configuration Manager
b.)Resource Arbitrator
c.)PCI Bus

d.)Device Driver

3.) Which component is not utilized by Plug and Play on a hardware level?

a.)DMA channels
b.)I/O devices
c.)DIP switches
d.)IRQs

4.) Which component creates an enumeration of the devices present on the machine?

a.)Utility Manager
b.)Configuration Manager
c.)Device Drivers
d.)Jumpers

5.) All of these are instrumental components of Plug and Play except:

a.) Device Hardware
b.) Operating System
c.) BIOS
d.) ISA Bus

Key: C, D, C, B, D

Multiple choice questions (Makai-Parrill-Rommel-Winfield: AMD-64, IA-32e Extensions, and IA-64 Architecture):

1. ***Through what modes do the AMD64 extensions achieve backwards compatibility?***
   a. ***It does not support backwards compatibility.***
   b. ***The AMD64 extensions achieve backwards compatibility by running in two separate modes, legacy mode and long mode.***
   c. ***The AMD64 extensions achieve backwards compatibility by running in two separate modes, short mode and long mode.***
   d. ***By magic.***

2. ***What was Intel's goal when it created the IA-32e 64-bit extensions?***
   a. ***Intel's goal when it created the IA-32e 64-bit extensions was to compete with the Itanium processor.***
   b. ***Intel's goal when it created the IA-32e 64-bit extensions was to bankrupt AMD and achieve a monopoly.***
   c. ***Intel's goal when it created the IA-32e 64-bit extensions was to maintain legacy support while also extending the x86 architecture.***
   d. ***All of the above.***

3. ***What is the main purpose of a 64-bit architecture?***
   a. ***The main purpose of a 64-bit architecture is to increase the maximum theoretical memory address to 16 exabytes.***
   b. ***The main purpose of a 64-bit architecture is to store more information on the hard drive.***
   c. ***The main purpose of a 64-bit architecture is to increase clock speed.***

d. The main purpose of a 64-bit architecture is to make the underlying processor more efficient

4. What was a problem with the original Itanium processor?
a. It had a slow integer processing speed.
b. The L2 cache was too small for practical use.
c. It was not directly backwards compatible without running the processor in much slower legacy mode.
d. People confused the name with Titanium.

5. Which of the two architectures discussed are best for workstation or server applications?
a. AMD64 and IA-32e
b. AMD64 and Itanium
c. Itanium and IA-32e
d. None of the above.

Correct answers: 1. b, 2. c, 3. a, 4. c, 5. b

Multiple choice questions (French-Kareem-Stancu-Tran: VAX-11):

1) The four access modes that memory management of the VAX architecture uses are?

a) general, executive, supervisor, and user
b) kernel, executive, supervisor, and user <Correct>
c) kernel, executive, manager, and user
d) kernel, executive, supervisor, and worker

2) The VAX has extended the PDP-11's virtual address space to a ____ virtual address.

a) 16-bit
b) 32-bit <Correct>
c) 64-bit
d) 16 byte

3) How many addressing modes does the VAX-11 Architecture support?

a) 32
b) 64
c) 16 <Correct>
d) 128

4) Which is not a floating-point integer format?
a) D_format
b) E_format <correct>
c) G_format
d) H_format

5) Who designed the VAX-11 Architecture?
a) DEC <correct>
b) IBM

c) Compaq
d) Dell

NOTE: The following questions are of questionable utility: they are either NOT multiple-choice (instructions explicitly stated that they MUST be multiple-choice), or the correct answers were not indicated (in-class instructions were that correct answers must be indicated:

(Drown-Rodden: RAID):

1. *Why isn't RAID 0 a true RAID level?*
   A. *It does not provide any redundency for fault tolerance.*

2. *What level is the most popular?*
   A. *Level 5*

3. *What does RAID stand for?*
   A. *Redundant Array of Inexpensive (or Independant) Disks*

4. *What is the name of the method, utilized in RAID, where multiple drives are partitioned and concantenated in an alternating pattern?*
   A. *Striping*

5. *What is the name of the method that spreads data across multiple drives to ensure fault tolerance?*
   A. *RAID*

Exam Questions (Ryan-Garcia-Wilkinson-Ripley: FireWire):

1.How many pins does a FireWire cable have if the device(s) DO NOT need a power bus?

Possible answers
- *2*
- *3*
- *4*
- *5*
- *6*

2.How many pins does a FireWire cable have if the device(s) DO need a power bus?

Possible answers

·2
·3
·4
·5
·6

3.What is the IEEE number for the most recent FireWire standard?

Possible answers
·0000e
·1111g
·2222l
·4444e
·1394b

4.FireWire is faster than which of the following device interconnections?

Possible answers
·Serial
·Parallel
·USB 1.1
·All of the above
·None of the above

5.FireWire is:

Possible answers
·A processor
·Fast cable interconnect
·Computer game
·Chipset
·File transfer program

(Bowman-Jones-Hall: DRAM):

What is Extended Data Out (EDO) DRAM also referred to as? -Hyper Page Mode DRAM -Ordinary Everyday (OED) DRAM -SDRAM

Fast Page Mode (FPM) DRAM has increased speed and lower power requirements when compared to conventional DRAM.
True/False

What was the first type of DRAM that kept in Sync with the computer Clock Speed?
SDRAM

At what speeds did the BEDO DRAM run at?

Ranges from 40 to 66 MHz

How are CAS2 chips better than CAS3 chips?

Allow to run faster when being overclocked

DDR-SDRAM is short for?

Double Data Rate-Synchronous DRAM

Dynamic Data Rate-Synchronous DRAM

Dual Data Rate-Synchronous DRAM

First generations DDR-SDRAM reached speeds of?

100 MHz - 133 MHz

266 MHz - 300 MHz

333 MHz - 400 MHz

Second generations DDR-SDRAM reached speeds of?

100 MHz - 133 MHz

333 MHz - 400 MHz

400 MHz and above

Single RDRAM data transmission?

512 KB

1 MB

1.6 GB