Last four digits of your JMU ID Number: ___ ___ ___ ___

NOTE: TO obtain credit for your performance in this exam, you must do all of the following: (1) Select one of the specified choices for multiple-choice questions (do NOT fill in the actual value of your answer, but instead indicate the lettered choice corresponding to it). (2) Sign the Honor Code declaration. (3) Wherever applicable, show your work.

CS-350: Computer Organization

Spring 2003: Quiz # 7 ANSWERS

1. In the following figure, part (a) is the summary diagram describing the entire device, while part (b) provides the detailed circuitry for the Enable Logic that determines when the register is loaded; the eight address lines are labeled $\mathbf{A_0}$ **. .** $\mathbf{A_7}$. What is the numeric address in hexadecimal assigned to this output device? *2 pts*

(Diagram deleted)

2. List all ***RTL*** operations implied in the following diagram. *8 pts*

(Diagram deleted)

Question	Answer
1	**F0** (AND gate requires 1s for A_7 . . A_4, and NOR gate requires 0s for A_3 . . A_0
2	**h: R←M** (j'•n'•o' results in selection of Mux input 0 (**M**); **h** causes **R** to load)
	j: M←A (j•n'•o' results in selection of Mux input 1 (**A**); **j** causes **M** to load)
	n: M←Y (j'•n•o' results in selection of Mux input 3 (**Y**); **n** causes both **M** and **Y** to load) **n: M←Y,Y←Y** is also an acceptable answer.
	o: A←R (j'•n'•o results in selection of Mux input 2 (**R**); **o** causes **A** to load)