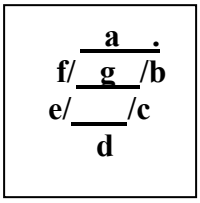
CS-350: Computer Organization

Spring 2003: Quiz # 3 ANSWERS

The following questions all relate to the Boolean Function corresponding to segment ***d*** of a seven-segment decoder. For each numbered question, fill in the lettered choice that corresponds to your answer.



(1) Consider the crude "Product of Sums" circuit implementation for the segment ***d*** decoder. For this first circuit implementation, do **NOT** employ any circuit simplification techniques. This circuit will be composed of NOT gates, OR gates, and an AND gate. How many transistors are there in the circuit?

3 pts

Answer: First, it is necessary to obtain the Truth Table for the specified segment. Next, pick out the rows whose values are zero: rows 1, 4, 7, and possibly also row 9 (see explanatory comment in the expanded table below).The minterms corresponding to these terms are: **W'X'Y'Z, W'XY'Z', W'XYZ,** and **WX'Y'Z.** The "OR" of these minterms constitutes the ***inverse*** of the Boolean function for segment ***d.*** In order to obtain the function itself, rather than its inverse, we need to invert the inverse, using DeMorgan's Theorems. The inverse of the OR of the four "product" terms consists of the AND of the inverses of the individual terms. These are the four MAXTERMs shown in the table below. The "Product of Sums" circuit consists of the AND of the three or four MAXTERMs.

Truth Table						**MAXTERMs in the function**
Numeric:	**W**	**X**	**Y**	**Z**	**Function for segment *d***	
0	0	0	0	0	1	
1	0	0	0	1	0	W + X + Y + Z'
2	0	0	1	0	1	
3	0	0	1	1	1	
4	0	1	0	0	0	W + X' + Y + Z
5	0	1	0	1	1	
6	0	1	1	0	1	
7	0	1	1	1	0	W + X' + Y' + Z'
8	1	0	0	0	1	
9	1	0	0	1	**0 or 1**	W' + X + Y + Z'
A	1	0	1	0	X	
B	1	0	1	1	X	
C	1	1	0	0	X	
D	1	1	0	1	X	
E	1	1	1	0	X	
F	1	1	1	1	X	

The display for the numeral 9 can either include or exclude segment ***d.*** Therefore, either a 0 or a 1 is acceptable in describing the Boolean function for segment ***d*** for the case where the input corresponds to the numeral 9.

If we include row 9 (i.e., row 9 is assigned a Boolean value of 0), then the crude "Product of Sums" circuit contains:

4 4-input OR gates @ 10 T = 40 Transistors
1 4-input AND gate @ 10 T = 10 Transistors
4 NOT gates @ 2T = 8 Transistors
TOTAL **58 Transistors**

However, if we exclude row 9 (i.e., row 9 is assigned a Boolean value of 1), then the crude "Product of Sums" circuit contains:

3 4-input OR gates @ 10 T = 30 Transistors
1 3-input AND gate @ 8T = 8 Transistors
3 NOT gates @ 2T = 6 Transistors (**W'** is not needed)
TOTAL **44 Transistors**

(2) Next, replace all the OR gates and the AND gate of this same circuit with NOR gates. How many transistors are there now in the circuit?

1 pt

Answer: The specified circuit transformation saves two transistors for each OR gate and for each AND gate in the original circuit. Therefore, net TOTAL = 58T – 10T = **48 Transistors** (including row 9),

or 44 T – 8 T = **36 Transistors** (excluding row 9)

(3) Next, consider the "Sum of Products" circuit, composed of NOT gates, AND gates, and an OR gate, that implements the functionality of the segment ***d*** decoder. Simplify this circuit as much as possible using the Karnaugh map circuit-simplification technique. How many transistors are there in the simplified "Sum of Products" circuit?

5 pts

Answer: There are two possibilities for the Karnaugh Map, corresponding to the two possible Boolean values for row 9 in the Truth Table for the function. For the case where row 9 contains a ***zero,*** the Karnaugh Map is

WX \ YZ	**00**	**01**	**11**	**10**
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	0	X	X

Marking two of the four groups:

WX \ YZ	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	0	X	X

These correspond,to **X'Z'** (the four corners) and **XY'Z**.
Another group corresponds to **X'Y:**

WX \ YZ	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	0	X	X

The last group corresponds to **YZ':**

WX \ YZ	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	0	X	X

Thus, the Karnaugh-Map-simplified Boolean **Function = X'Z' + YZ' + X'Y + XY'Z**. The transistor count is:

3 2-input AND gates @ 6 T	=	18 Transistors
1 3-input AND gate @ 8 T	=	8 Transistors
1 4-input OR gate @ 10T	=	10 Transistors
3 NOT gates @ 2 T	=	6 Transistors
TOTAL		**42 Transistors**

Next, consider how the Karnaugh Map looks when row 9 of the Truth Table is set to ***one*:**

WX \ YZ	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	1	X	X

This Karnaugh map contains the ***same*** four groups as the previous one, plus one additional group, whose value is **W'**:

WX \ YZ	**00**	**01**	**11**	**10**
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	1	X	X

Thus, the Karnaugh-Map-simplified Boolean **Function = X'Z' + YZ' + X'Y + XY'Z** + **W**. This results in the second-stage OR gate's being changed from 4-input to 5-input (2 additional transistors):

3 2-input AND gates @ 6 T = 18 Transistors
1 3-input AND gate @ 8 T = 8 Transistors
1 **5**-input OR gate @ 12T = 12 Transistors
3 NOT gates @ 2 T = 6 Transistors
TOTAL **44 Transistors**

(4) Finally, replace the AND gates and the OR gate of the simplified "Sum of Products" circuit with NAND gates. How many transistors are there now?

1 pt

Answer: The specified circuit transformation saves two transistors for each AND gate and for each OR gate in the original circuit. Therefore, net TOTAL = 42T – 10T = **32 Transistors** (row 9 = 0), ***or*** 44T – 10T + 2T (the last "+2T" because replacement of the second-stage OR gate with a NAND gate requires that we invert the **W** output to **W'** in compensation) = **36 Transistors** (row 9 = 1)

A	22
B	32
C	42
D	52
E	62
F	72
G	82
H	92
I	102
J	48
K	58
L	68
M	78
N	88
O	98
P	none of the above

Row 9 of the Truth Table = ***zero*****:**

Question	**Answer**
1	**K**
2	**J**
3	**C**
4	**B**

Row 9 of the Truth Table = ***one*****:**

Question	**Answer**
1	**P**
2	**P**
3	**P**
4	**P**

NOTE that ***all*** answers need to fit either the upper group (**K-J-C-B**) or the lower group (**P-P-P-P**).